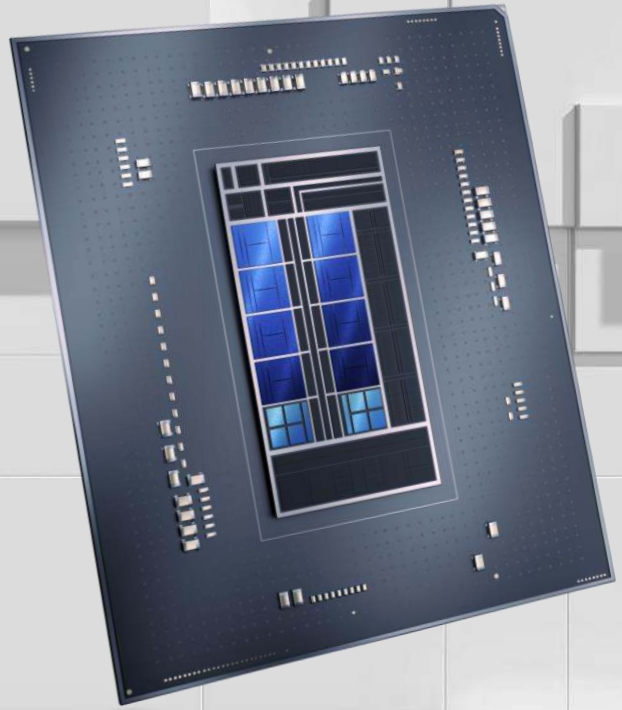
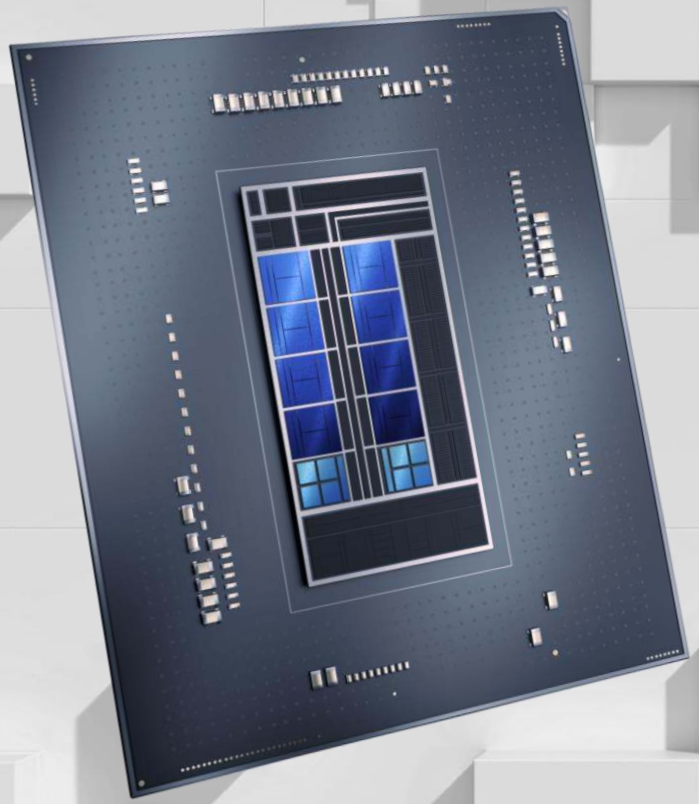
Alder Lake Architecture



Efraim Rotem, Yuli Mandelblat, Vadim Basin, Eli Weissmann, Arik Gihon, Rajshree Chabukswar, Russ Fenger, Monica Gupta

intel®

HOT CHIPS



Introducing

Alder Lake

Reinventing Multi Core Architecture

All-New Core Design

Built for Performance Hybrid

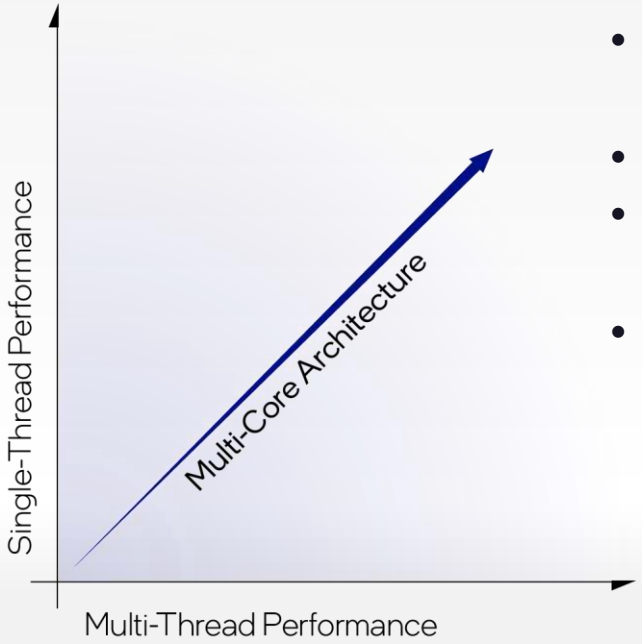
Single, Scalable SoC Architecture

All Client Segments – 9W to 125W – built on Intel 7 process

Intel Thread Director

Intelligence built into the Core

Alder Lake Performance Hybrid

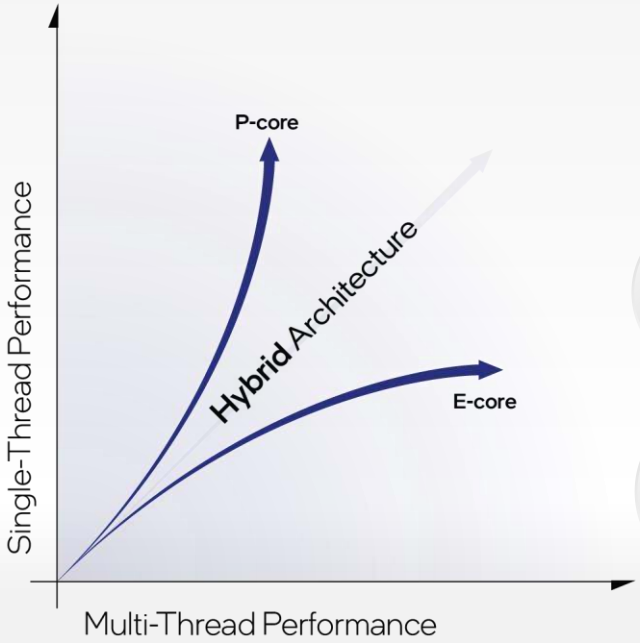


- Single Thread general purpose compute still critical
  - Low latency high IPC - ST and serial segments
- Support vector and ML instructions
- Drives size and power

- Increase in Parallel apps (MT)
  - Machine Learning/AI
  - Concurrent usage
  - Focus on user experience

Shift from multi-ST-performance cores → Performance Hybrid

Alder Lake Performance Hybrid

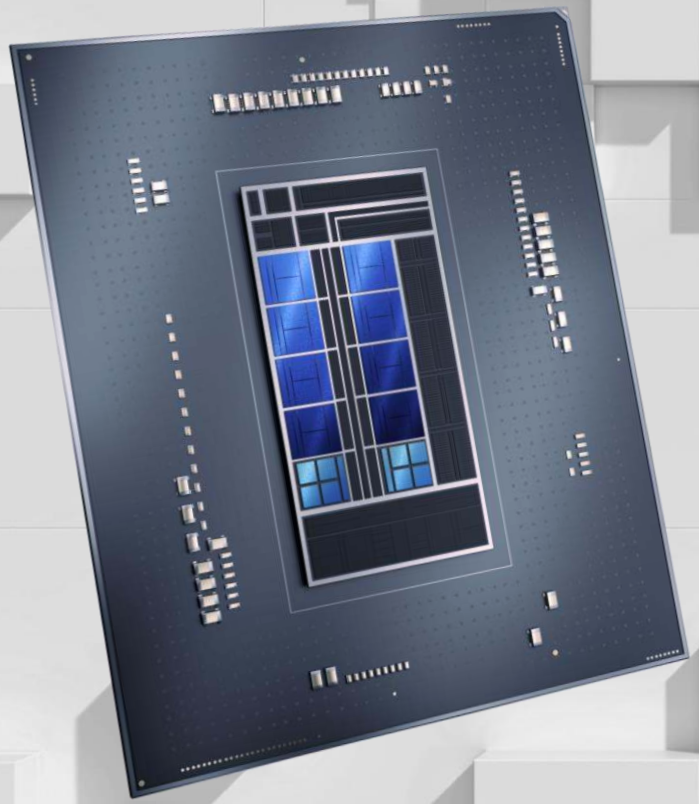


Same architecture
Different micro architecture
Different optimization and design point

P-core
Unleash the design to deliver even more ST performance

E-core
Created an efficient throughput machine

Performance Hybrid → E-cores deliver throughput P-Core deliver Performance



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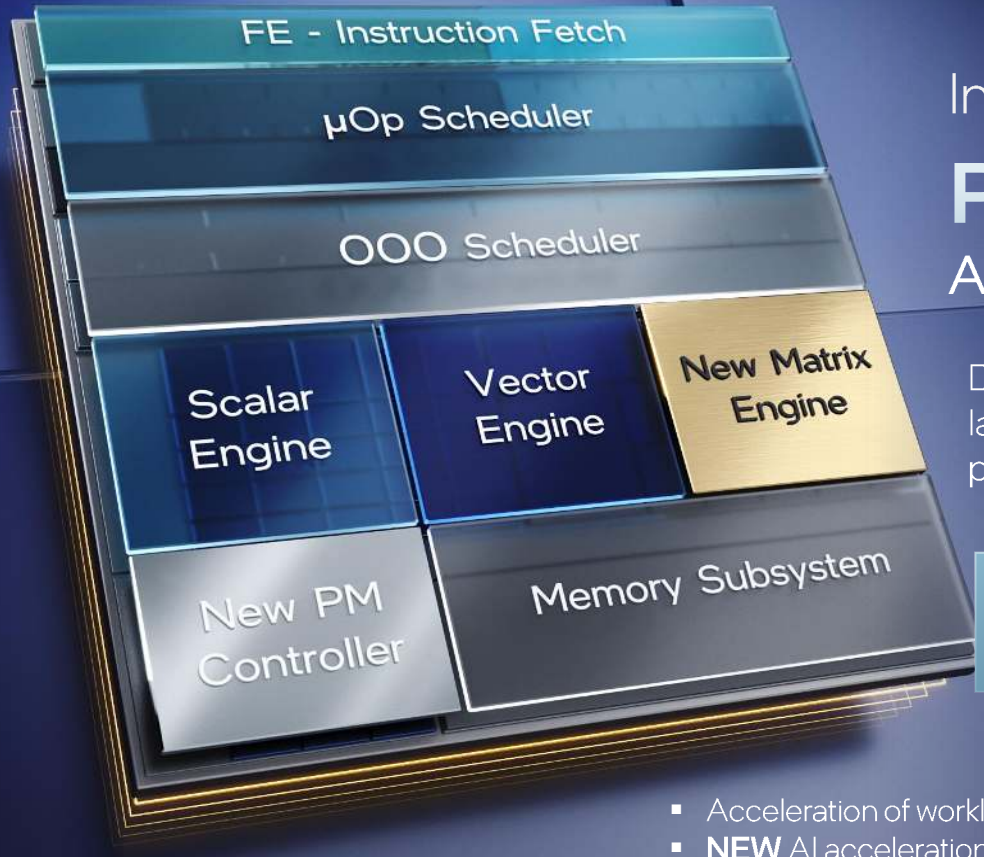
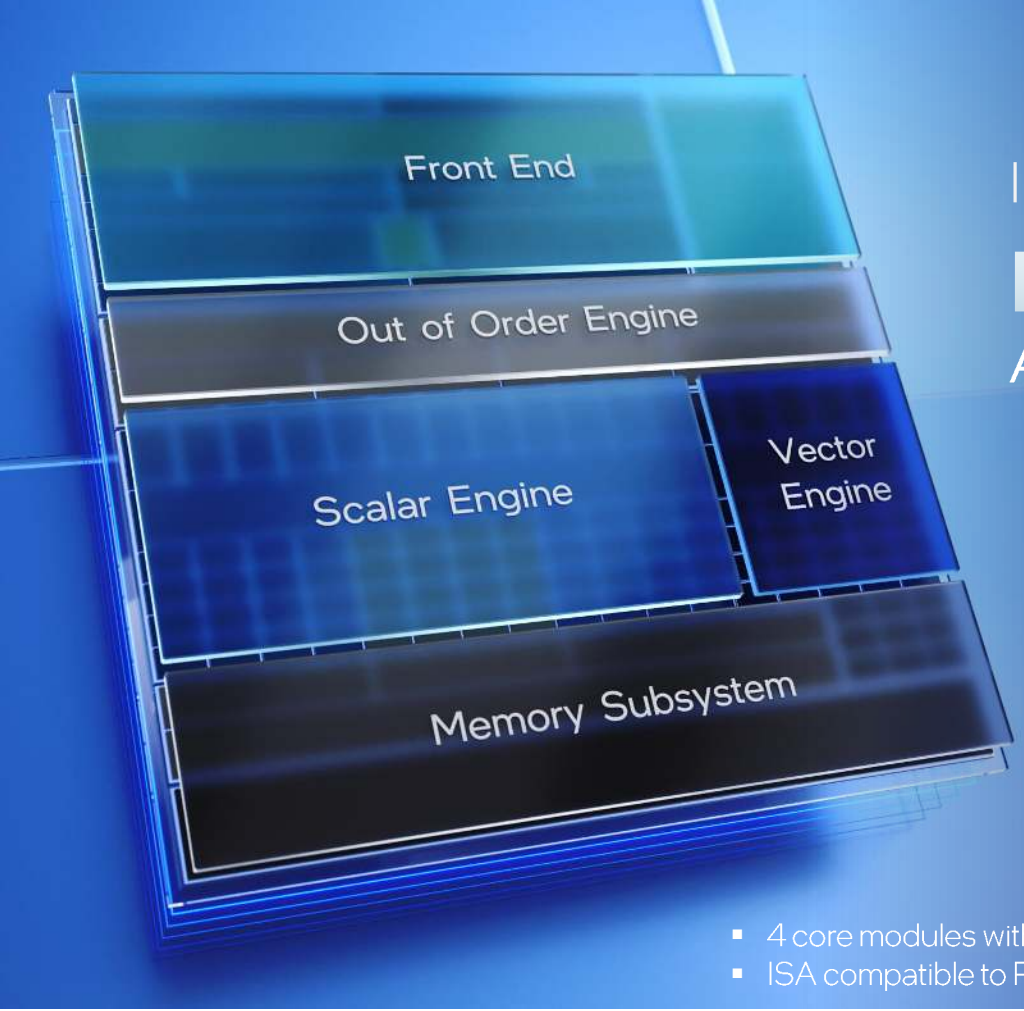


Intel's New **Performance** x86 Core Architecture

Designed for speed, pushing the limits of low latency and single threaded application performance via:

Wider | **Deeper** | **Smarter**

- Acceleration of workloads with large code footprint & large data sets
- **NEW** AI acceleration technology via coprocessor for matrix multiplication
- **NEW** smart PM controller for fine grain power performance management



Intel's New **Efficient** x86 Core Architecture

designed for throughput, enabling scalable multi-threaded performance for modern multi-tasking

Optimized for power and density efficient throughput with:

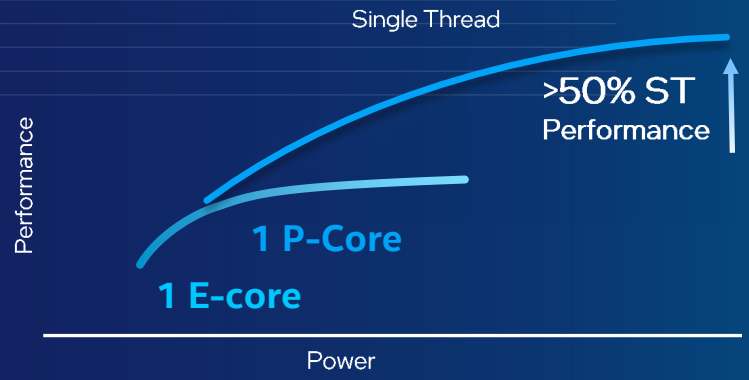
Deep Front-End
with on-demand length decode

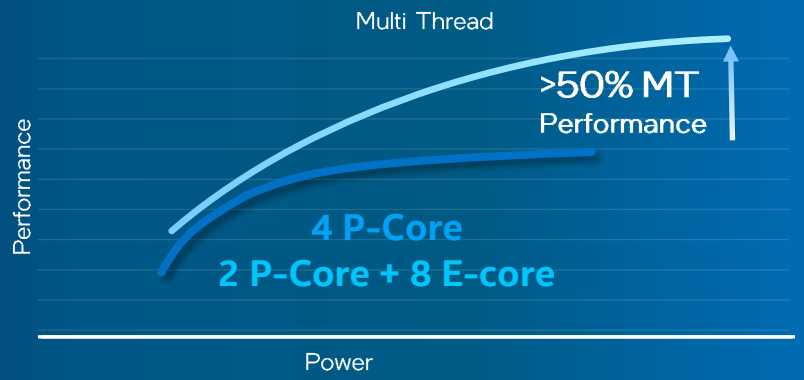
Wide Back-End
with many execution ports

Optimized Design
for latest transistor technologies

- 4 core modules with shared MLC for modularity of throughput compute
- ISA compatible to P-Core

E-Core To P-Core Performance Efficiency

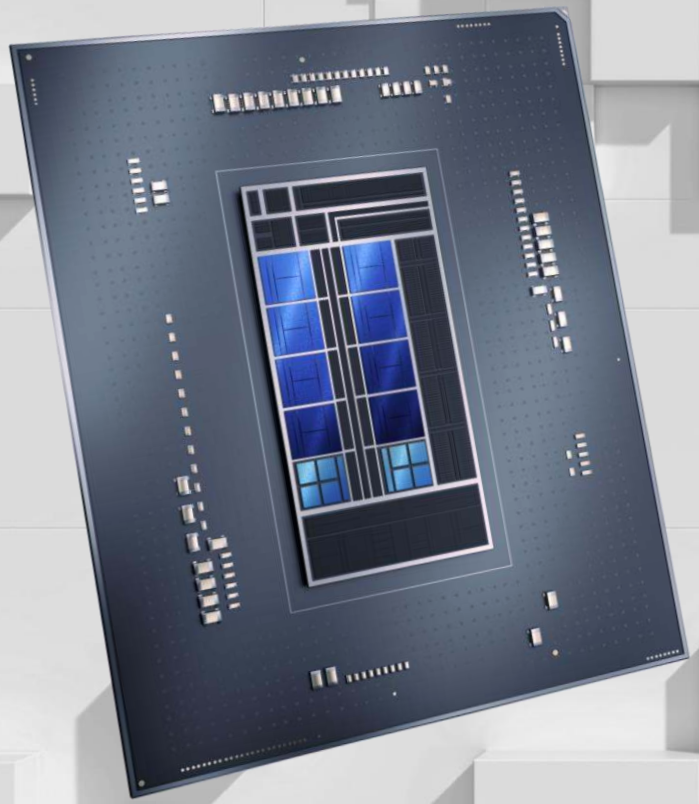




P-Core delivers higher Performance on single and lightly threaded scalable apps.

E-Core provide higher computational density under given physical constraints

Note: Charts are for illustrative purposes only



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Scalable Client Architecture

Ultra Mobile

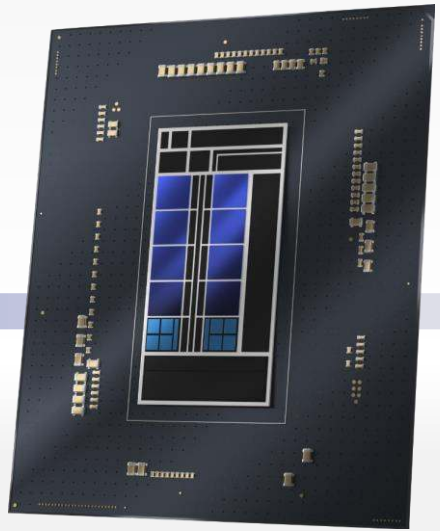
BGA Type4 HDI
28.5 x 19 x 1.1 mm

Mobile

BGA Type3
50 x 25 x 1.3 mm

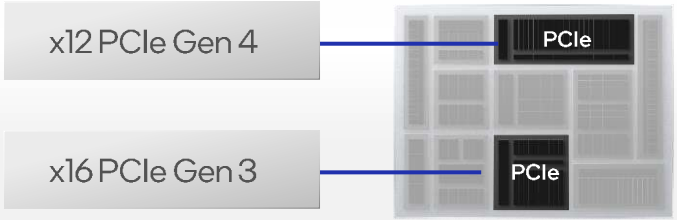
Desktop

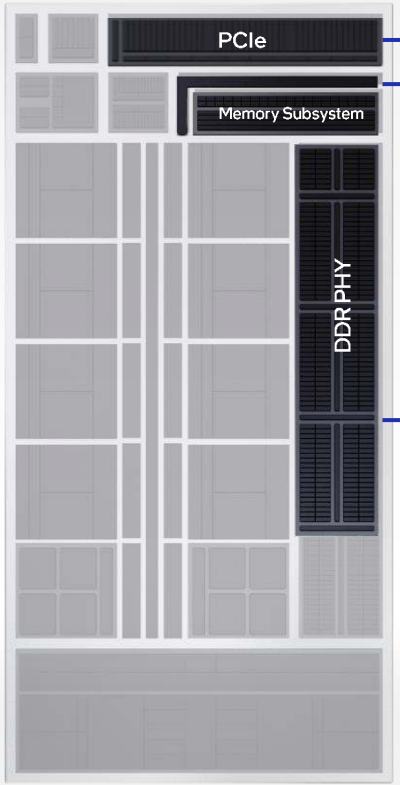
LGA 1700
Socket



Alder Lake I/O

Leading the industry transition to PCIe Gen5
Up to 2X bandwidth vs. Gen4
Up to 64GB/s with x16 lanes
Support for all four major memory technologies
Dynamic voltage-frequency scaling
Enhanced overclocking support

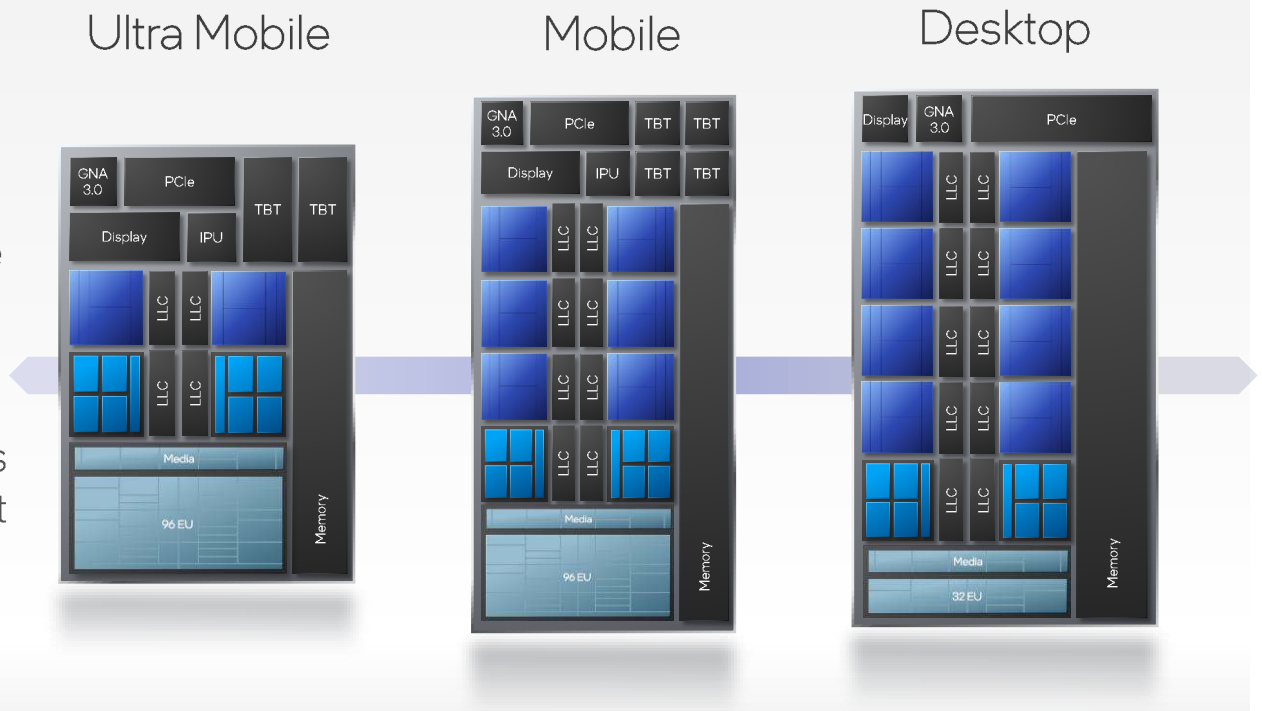




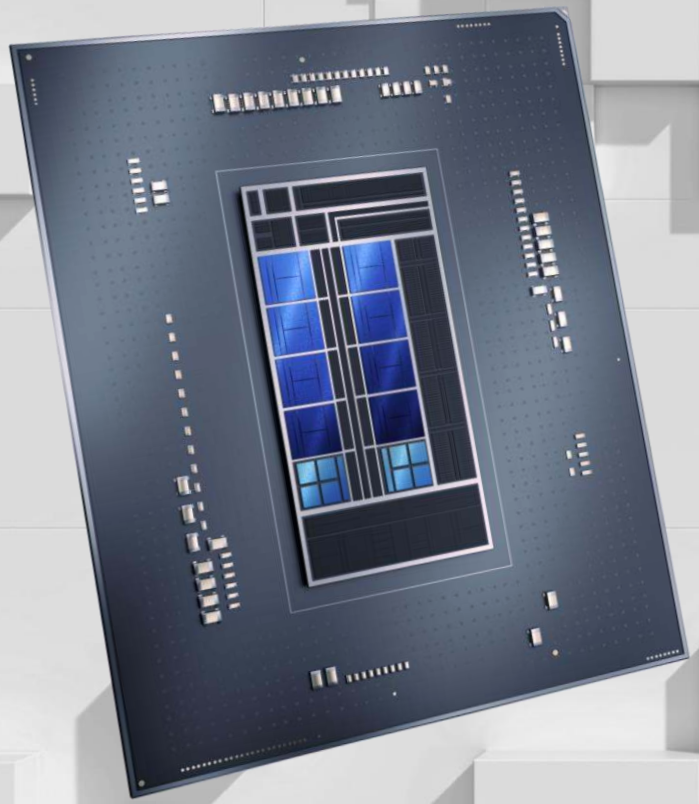
x16 PCIe Gen 5 — New
x4 PCIe Gen 4
Up to 64 GB/s I/O
Demand- based
DDR5 – 4800 — New
DDR4 - 3200
LP5 - 5200 — New
LP4x - 4266

All cores are exposed to OS
Logical processors accessible

Hybrid topology enumerated
No hard coded information
Same OS and SW for all builds
HW support and management



Building Blocks



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Intelligence built into the Core

Introducing

Intel **Thread Director**

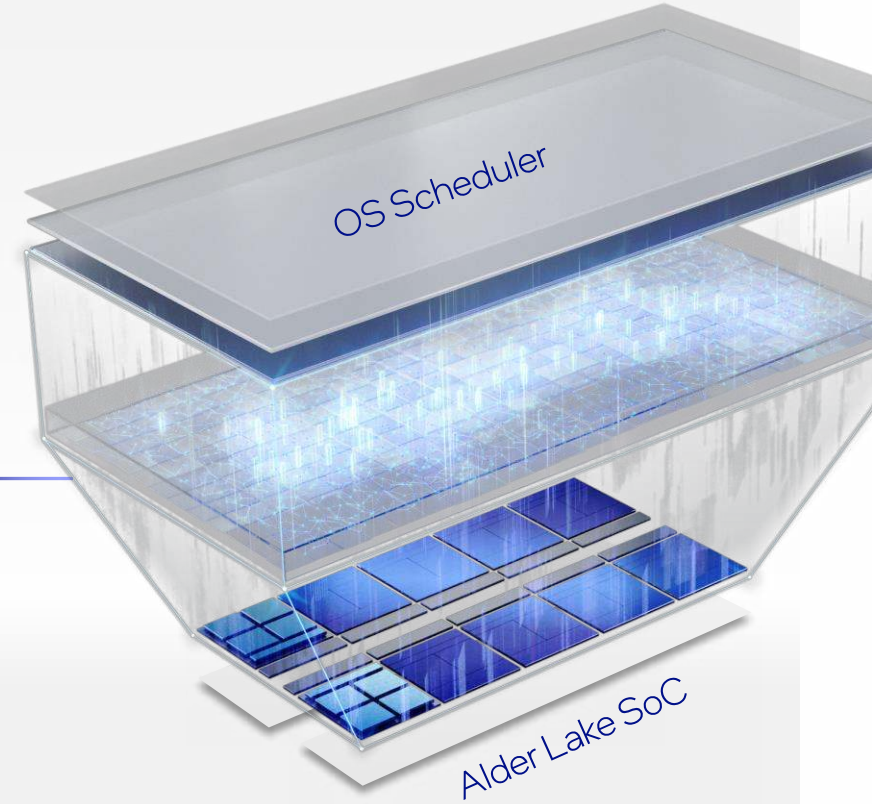
Intelligence built directly into the core

Monitors the runtime instruction mix
of each thread and as well as the state of each core – with nanosecond precisionv

Provides runtime feedback to the OS
to make the optimal scheduling decision for any workload or workflow

Dynamically adapts guidance
based on the thermal design point, operating conditions, and power settings – without any user input

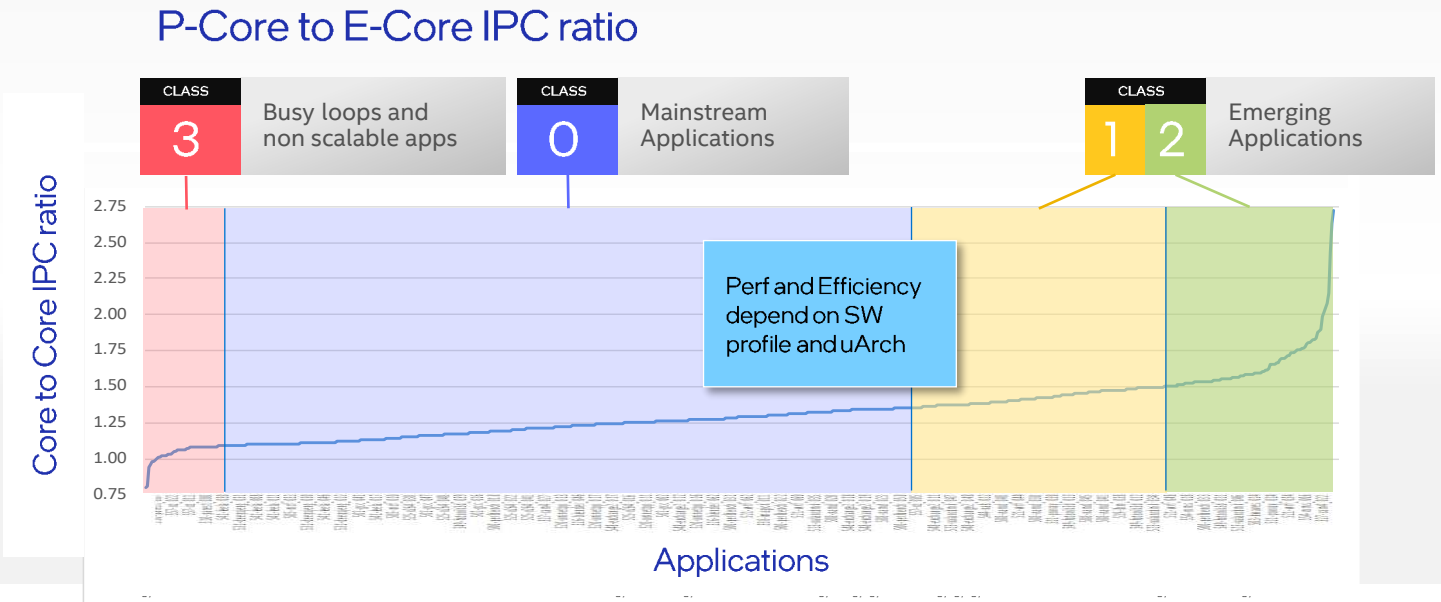
Power and energy management
Adjust Voltage and frequency to meet user experience while optimizing power, thermal and energy consumption



Intel **Thread Director -** Telemetry

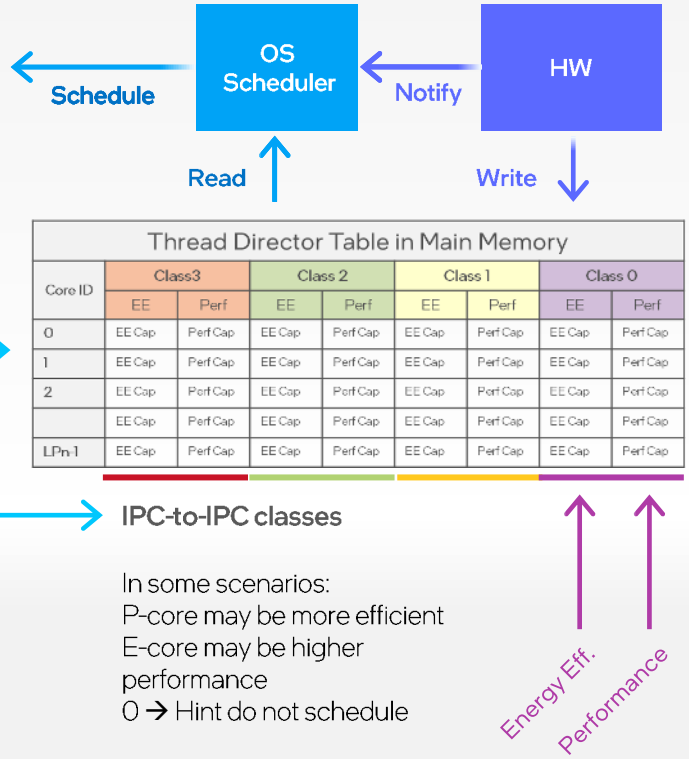
New Machine Learning based thread telemetry of core-to-core perf.

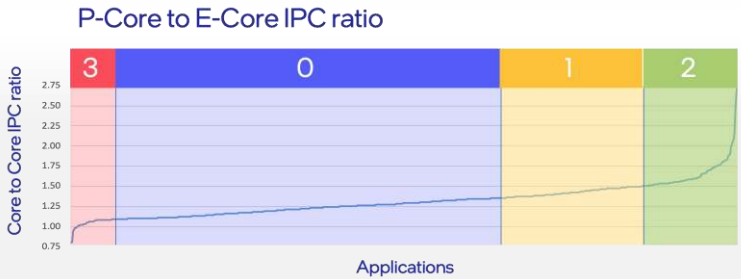
- Tunned and extensively validated
- IPC gain of P-core vs. E-core → attach class to thread architectural context



Intel **Thread Director** - Architecture

- HW periodically writes a feedback table (EHFI)
  - Function of aggregated load and physics
- OS scheduler selects the best core allocation for the SW thread runtime properties and class
  - Most performing core -or-
  - Most energy efficient core
  - Communicates Energy Performance Preference

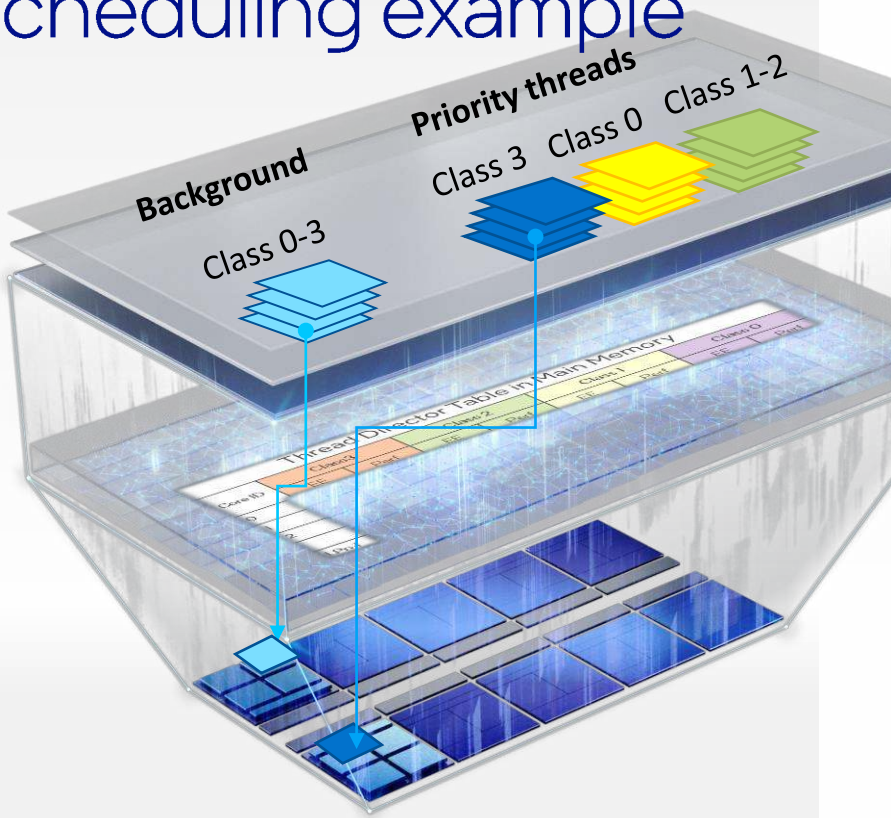




Intel **Thread Director** – Scheduling example

1. EHFI table enumerate core properties per class for the OS

2. Background threads of any class directed to energy efficient core



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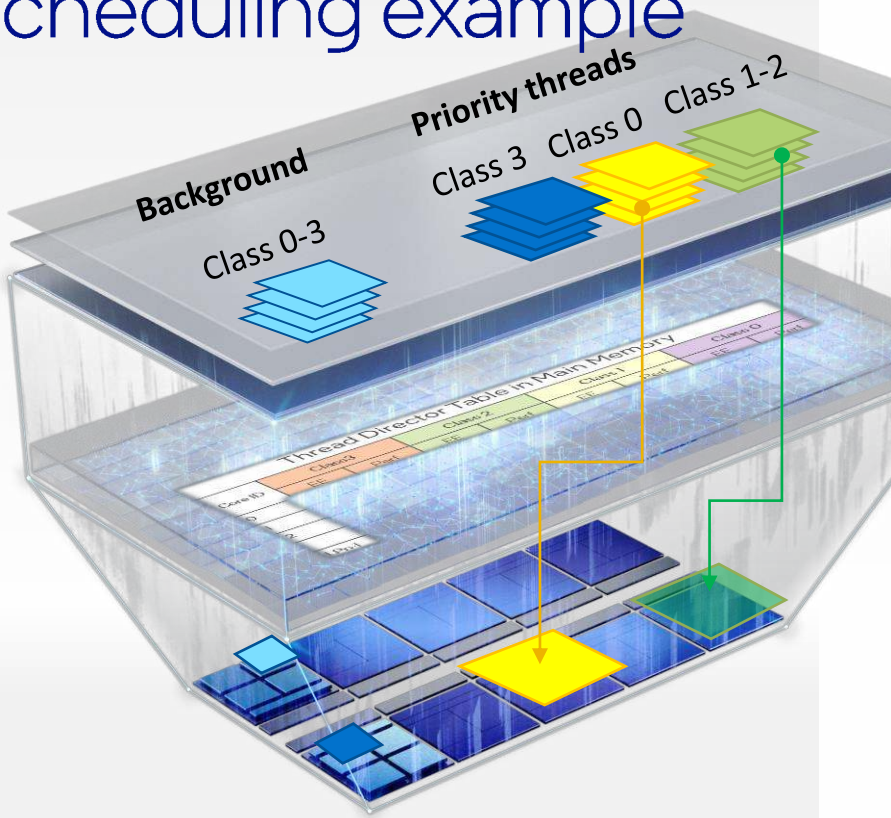
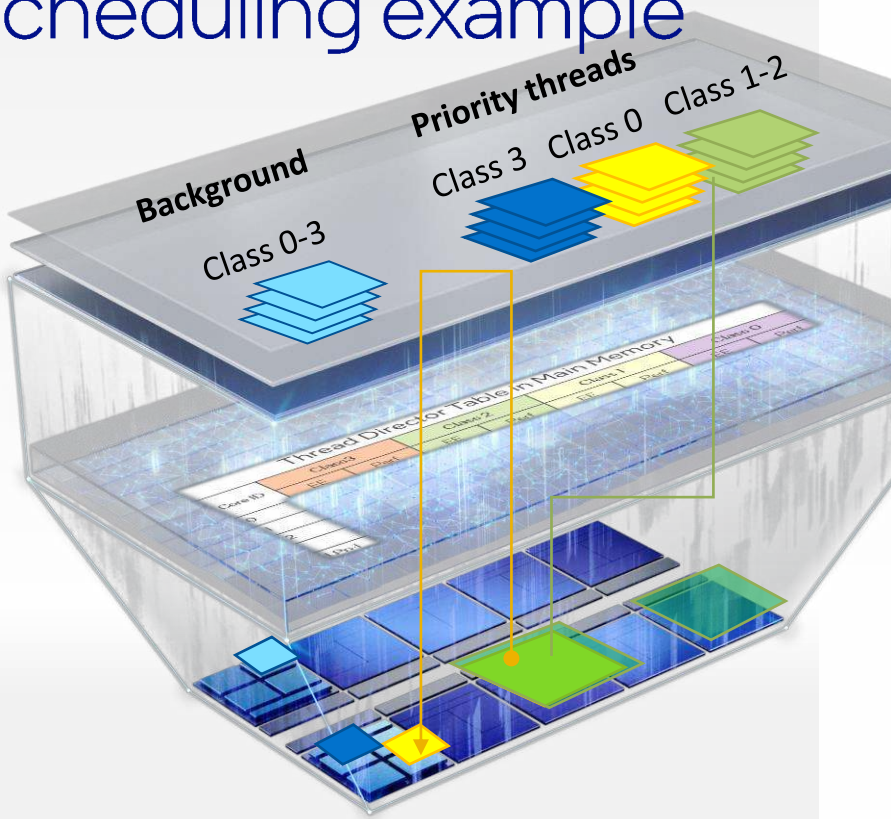


Intel **Thread Director** – Scheduling example

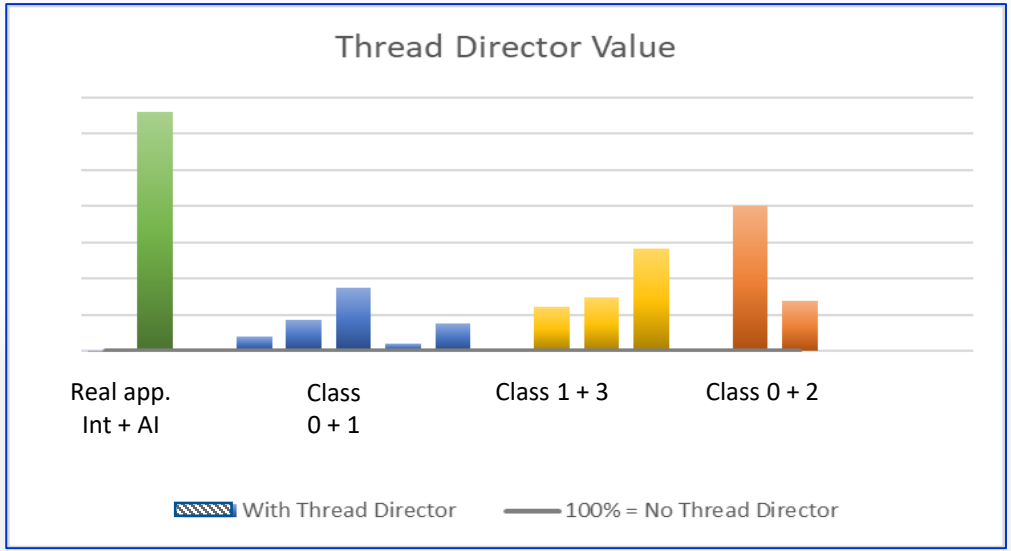
1. EHFI table enumerate core properties per class for the OS
2. Background threads of any class directed to energy efficient core
3. Priority threads are directed to performance cores
4. In case of contention on priority core, lower class will be moved for higher class



Intel **Thread Director** - Value

Performance with Intel Thread Director enabled vs. disabled

- Baseline is Alder Lake without Thread Director
- Placement of the right thread on the right core
- Impact real life application mix
  - Integer, Vector and AI
  - Background operations



*** Note: Chart is for illustrative purposes and not at scale**

Intel **Thread Director –** Power and energy

Alder Lake power management rearchitected - hybrid aware

- Core properties and topology
- Impacted by and controls thread scheduling

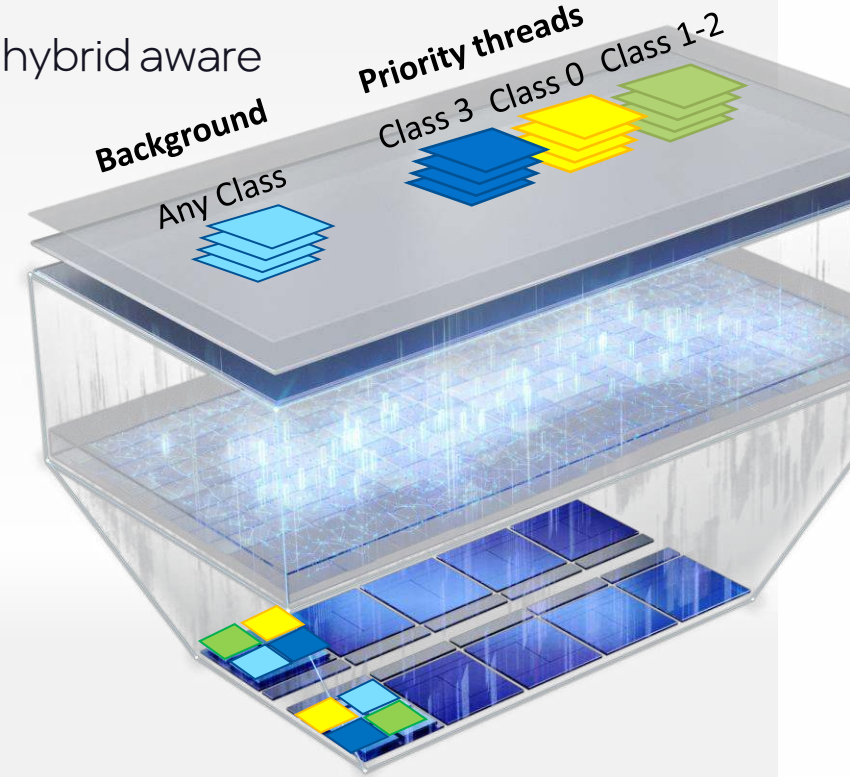
Example

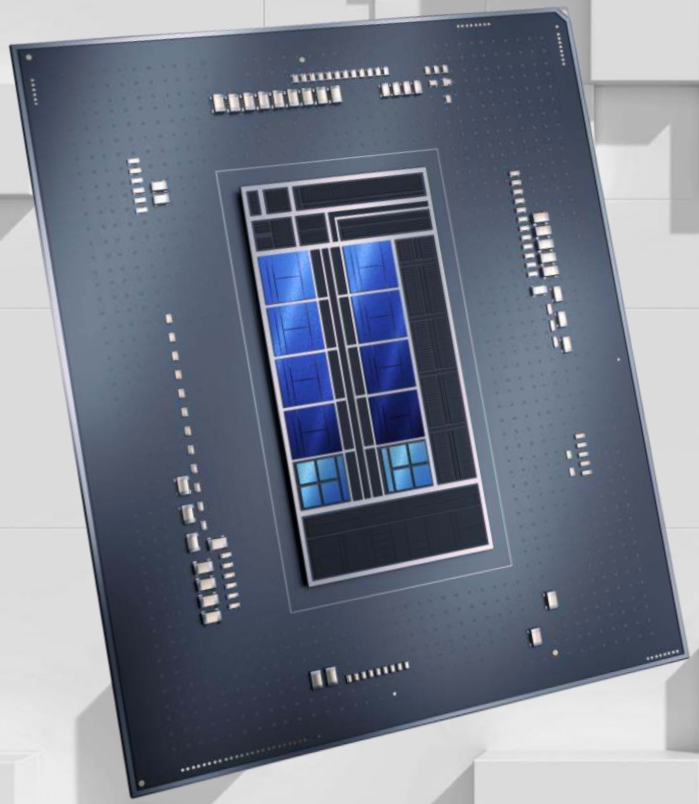
Each core type may run a mix of thread priorities

- Background threads → low frequency
- Priority threads → high frequency
- Frequency is balanced between core types
- Adjusted to compute load

On power constrained system → power balancing

- Power budget distribution optimized





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Thank you!

Fig. 1

Fig. 6

A powerful element,
a university, a turn.

bit.ly/2VEW6Dt