EDGE Q

5G WITH AN EDGE

SRIRAM RAJAGOPAL | HEAD OF SYSTEMS ENGINEERING

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EDGEQ

THE TEAM THAT POWERED THE MOBILE FIRST REVOLUTION

SRIRAM RAJAGOPAL
HEAD OF SYSTEMS DESIGN

- System Architect for Advanced Wireless Systems
- 10+ Issued Patents and 5 Conference Publications
- Distinguished Engineer at Altiostar Networks
- Head of PHY Layer Systems at Beceem Communications
- Stanford University (MSEE) | Univ of Madras (BE)

About EdgeQ

50+ SoCs Launched. 2Billion Modems Shipped

$100+B Revenue Generated

Modems Designed into all Apple/Android Products

DELIVERED 8+ GENERATIONS OF MODEMS TO THE MARKET

DISTINGUISHED WIRELESS PEDIGREE

Qualcomm intel BROADCOM

20+ YEARS OF 4G/5G AND ARTIFICIAL INTELLIGENCE EXPERTISE

LUMINARY ADVISORS

PAUL JACOBS
ex-CEO, Qualcomm

MATT GROB
ex-CTO, Qualcomm

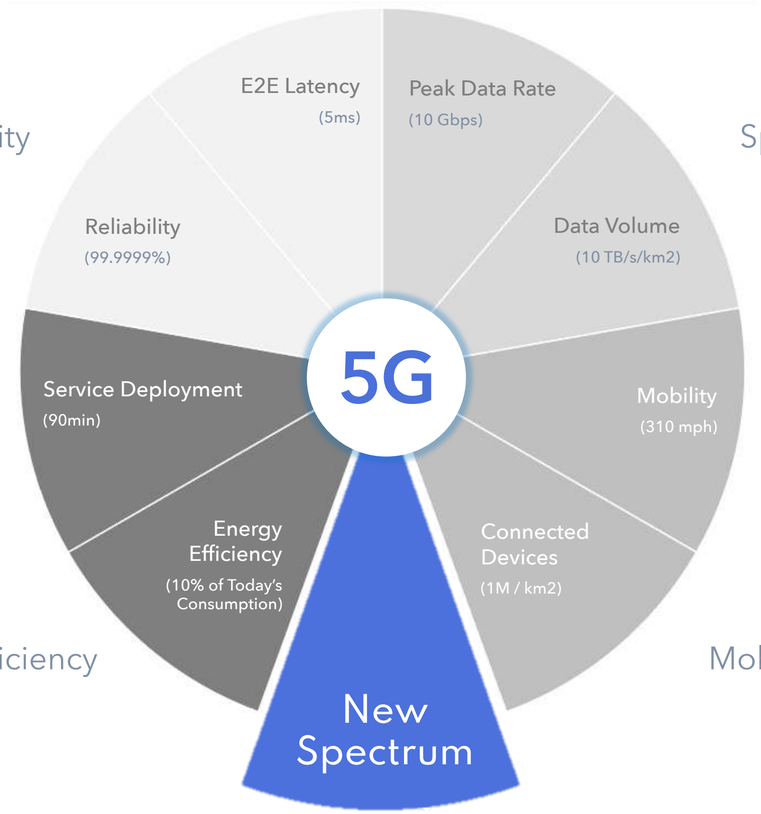
CHRISTOS KOZYRAKIS
Stanford University, EE Dept

What is 5G.

Enabling the Next Trillion “Users”

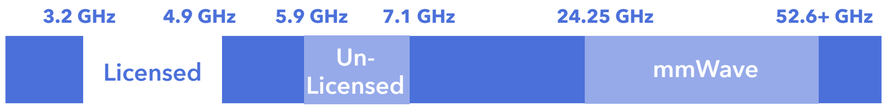
Latency / Reliability

Speed / Throughput

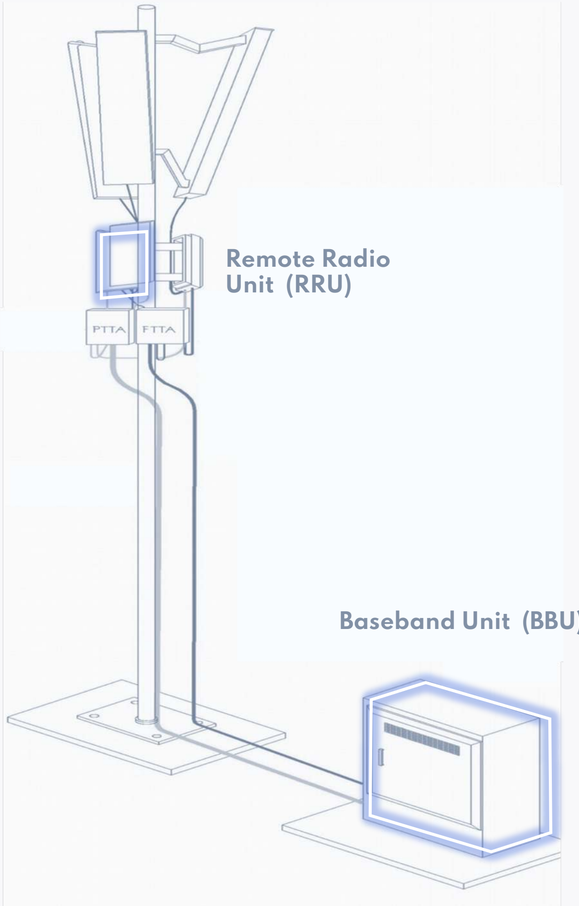


Deployment / Efficiency

Mobility / Connectivity



Progressions of 4G/5G Base Station Architecture



TRADITIONAL

Proprietary Hardware

Proprietary Interface

Proprietary Software

vRAN

Proprietary Hardware
with COTS Server

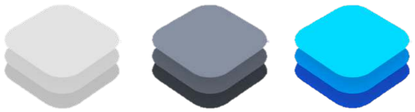
Proprietary Interface

Proprietary Software
with Virtualized Function

Open RAN

COTS-Based Hardware
(from any hardware vendor)

Open Interface

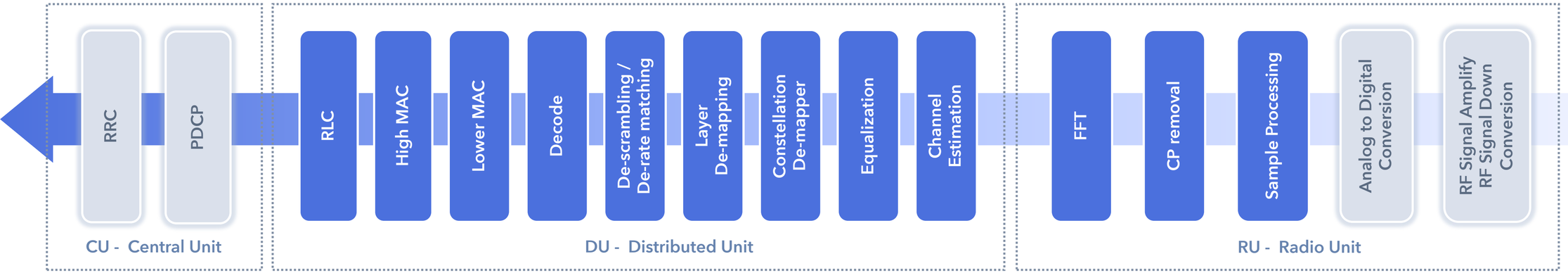


Software with Virtualized Function
(from any software vendor)

Open RAN = Virtualized Software + Open Interface Hardware

EDGEQ

O-RAN Base Station Under the Hood



X86 | ARM

Central Unit

OPEN INTERFACE

Mid-Haul

DSPs and x86 | ARM

Distributed Unit

OPEN INTERFACE

Front-Haul

DSPs and RF

Radio Unit

IP LEVEL PACKET PROCESSING
RADIO RESOURCE CONTROL

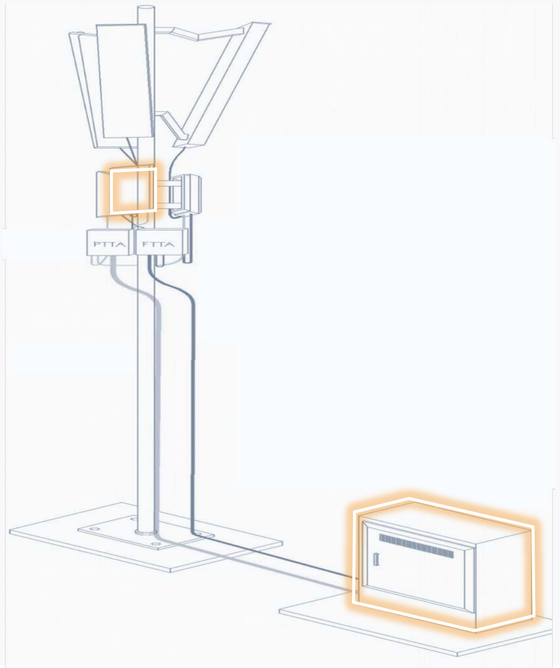
- General Purpose Hardware
- PDCP, RRC

SYMBOLS TO BITS
ERROR CORRECTIONS → BITS TO PACKETS

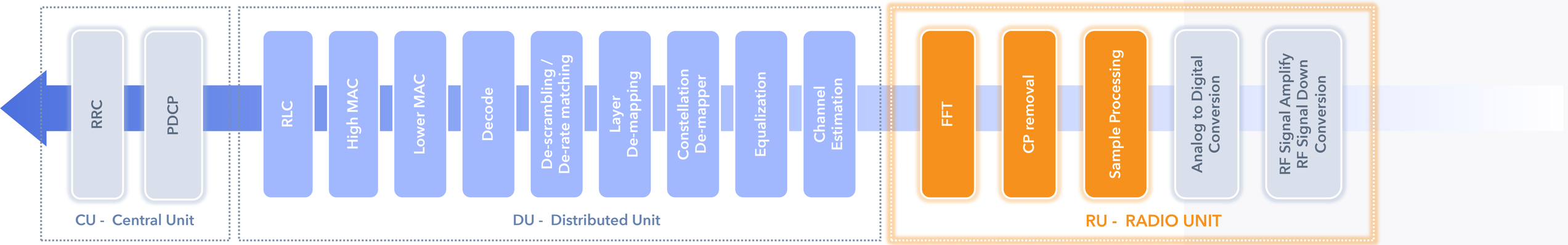
- Hybrid Hardware – specialized or general purpose
- Upper PHY
- MAC, RLC

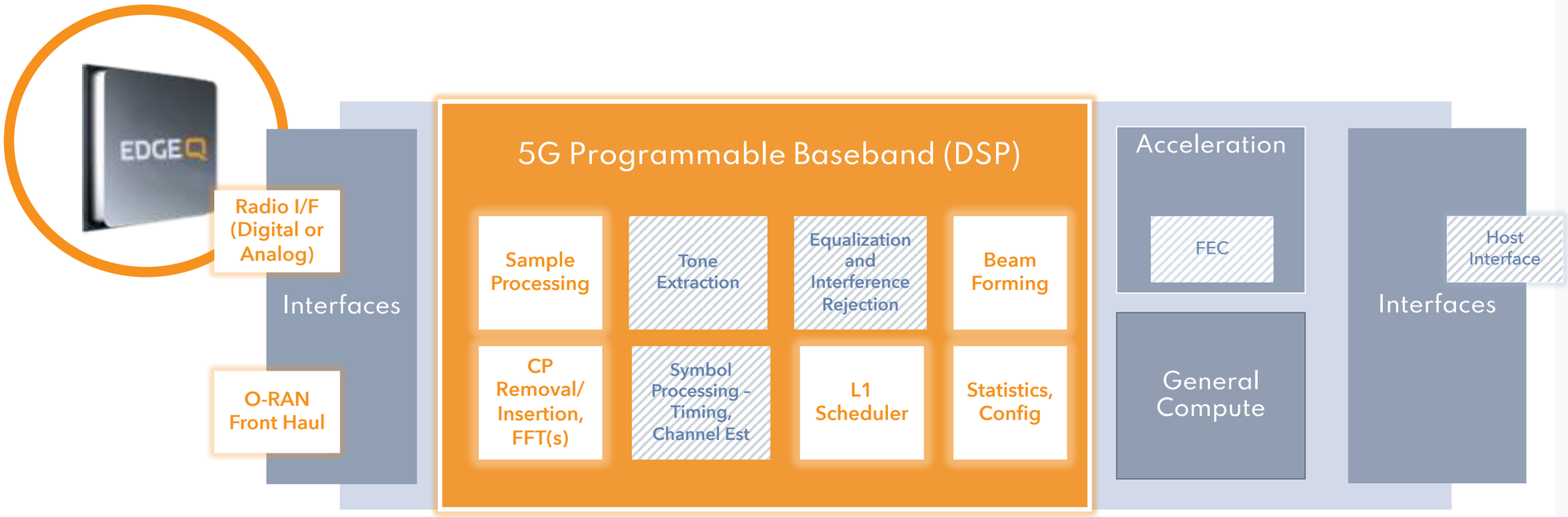
RF TO DIGITAL SAMPLES
SAMPLES → SYMBOLS

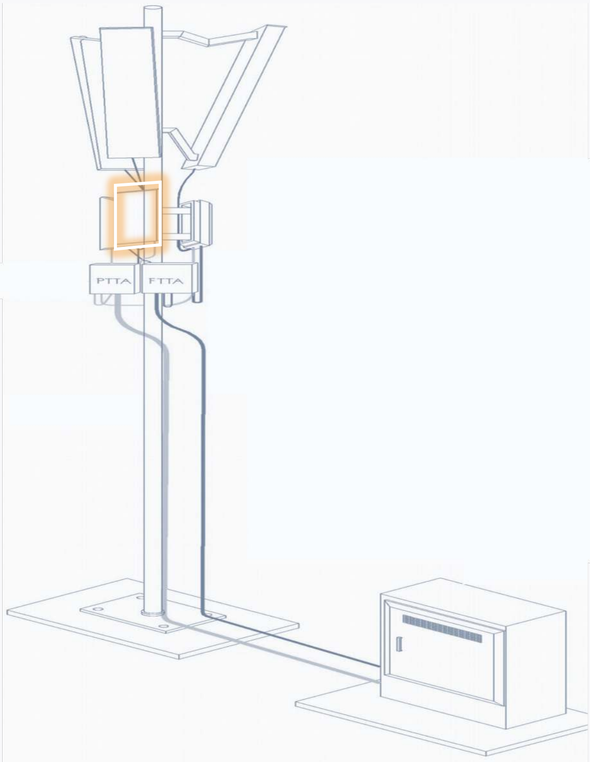
- Specialized Hardware
- Support for different Bands, Duplexing methods



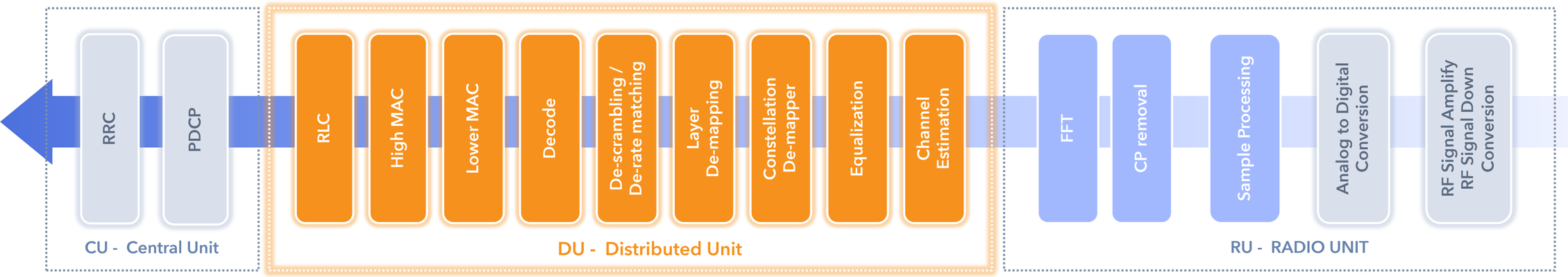
Converged 5G Physical Layer – RU Implementation

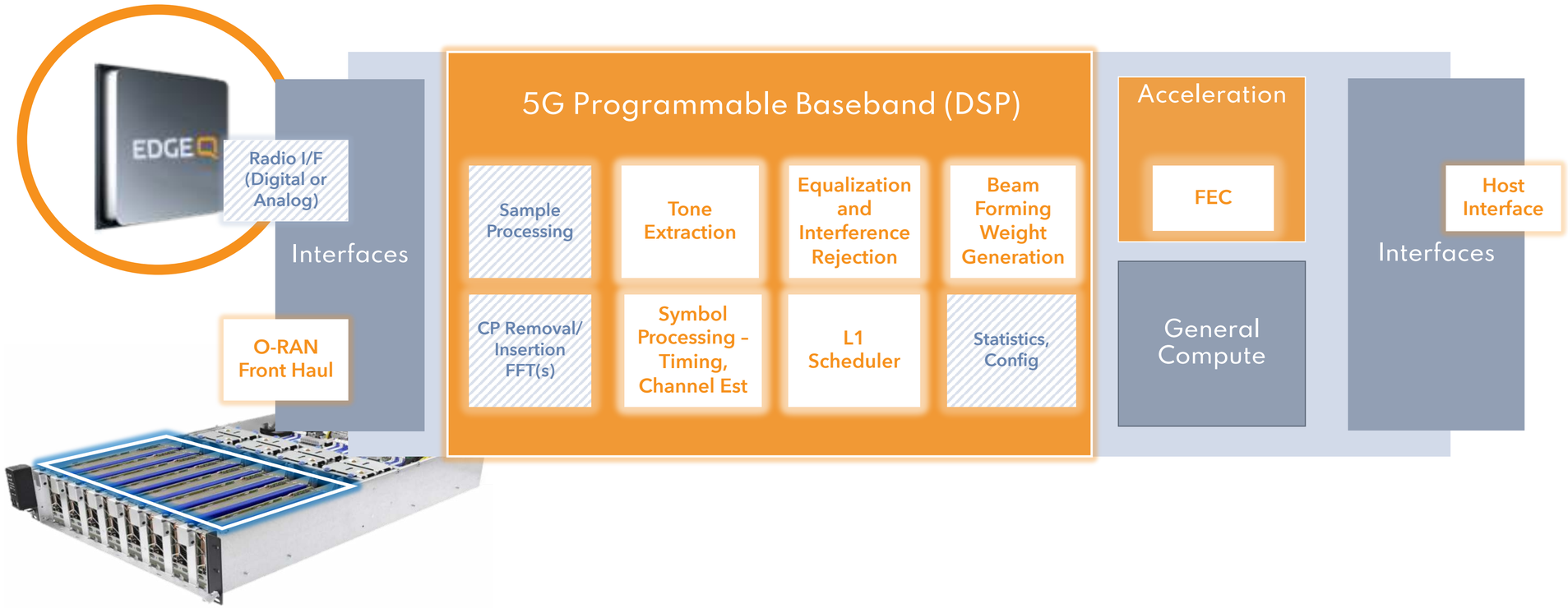


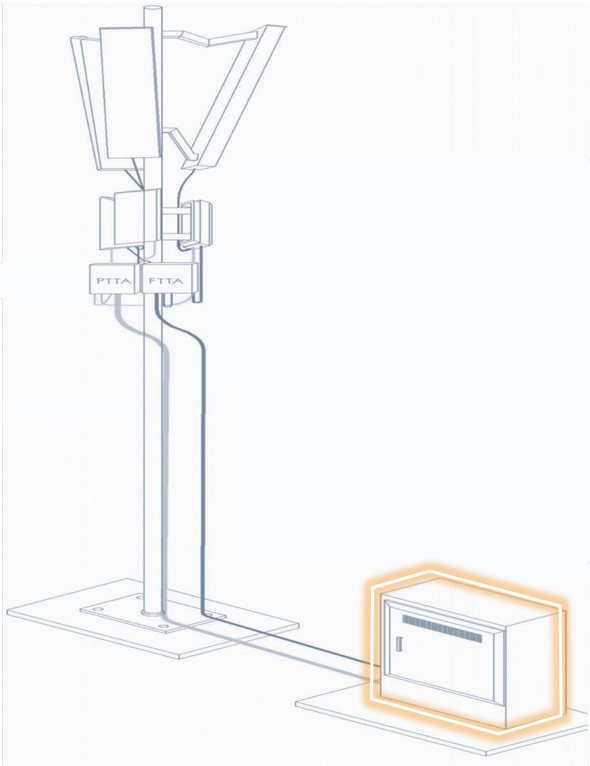




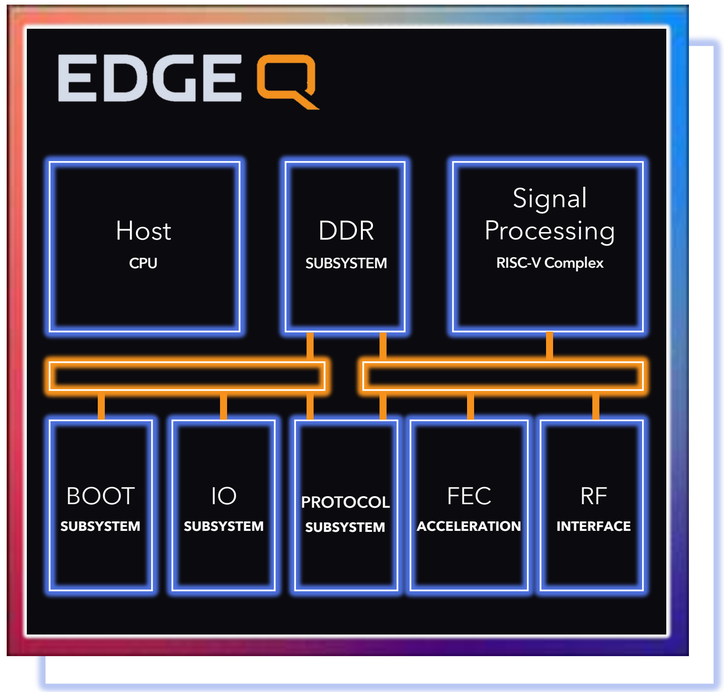
Converged 5G Physical Layer – DU Implementation

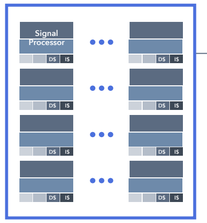






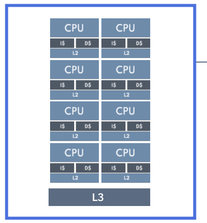
EdgeQ 5G Base Station-on-a-Chip





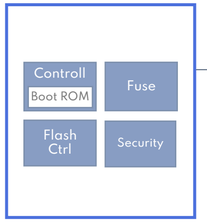
Signal Processing Complex

Specialized Baseband Processor RISC-V ISA including 50+ custom instructions and extensions



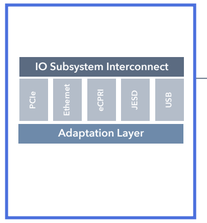
CPU Subsystem

Eight-core ARM Neoverse CPU Cluster for service provisioning and data processing



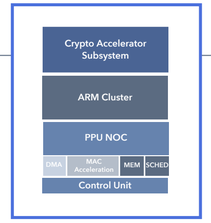
Boot Subsystem

Secure Boot Up via NOR / SPI/ NAND, Flash controller, Root of Trust Stored



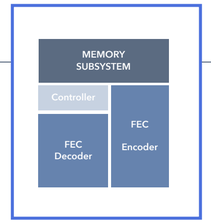
IO Subsystem

Controllers for PCIe, USB, Ethernet, eCPRI, JESD, Inter-chip



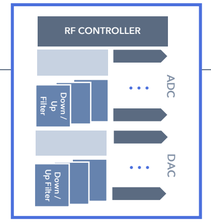
Protocol Accelerator

L2/L3 Accelerators for MAC and Cryptographic Processing



FEC Acceleration

Forward Error Correction (FEC) Engines and Bit Processing for 4G/5G



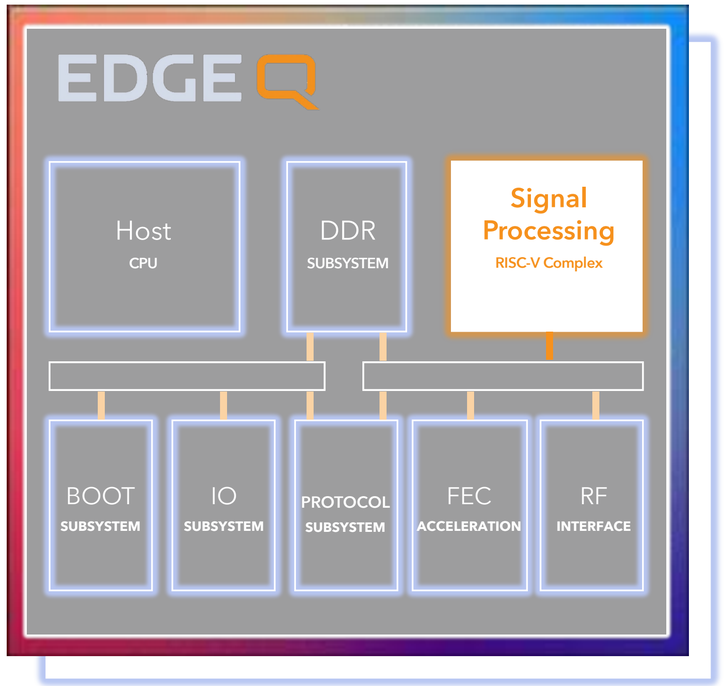
RF Interface

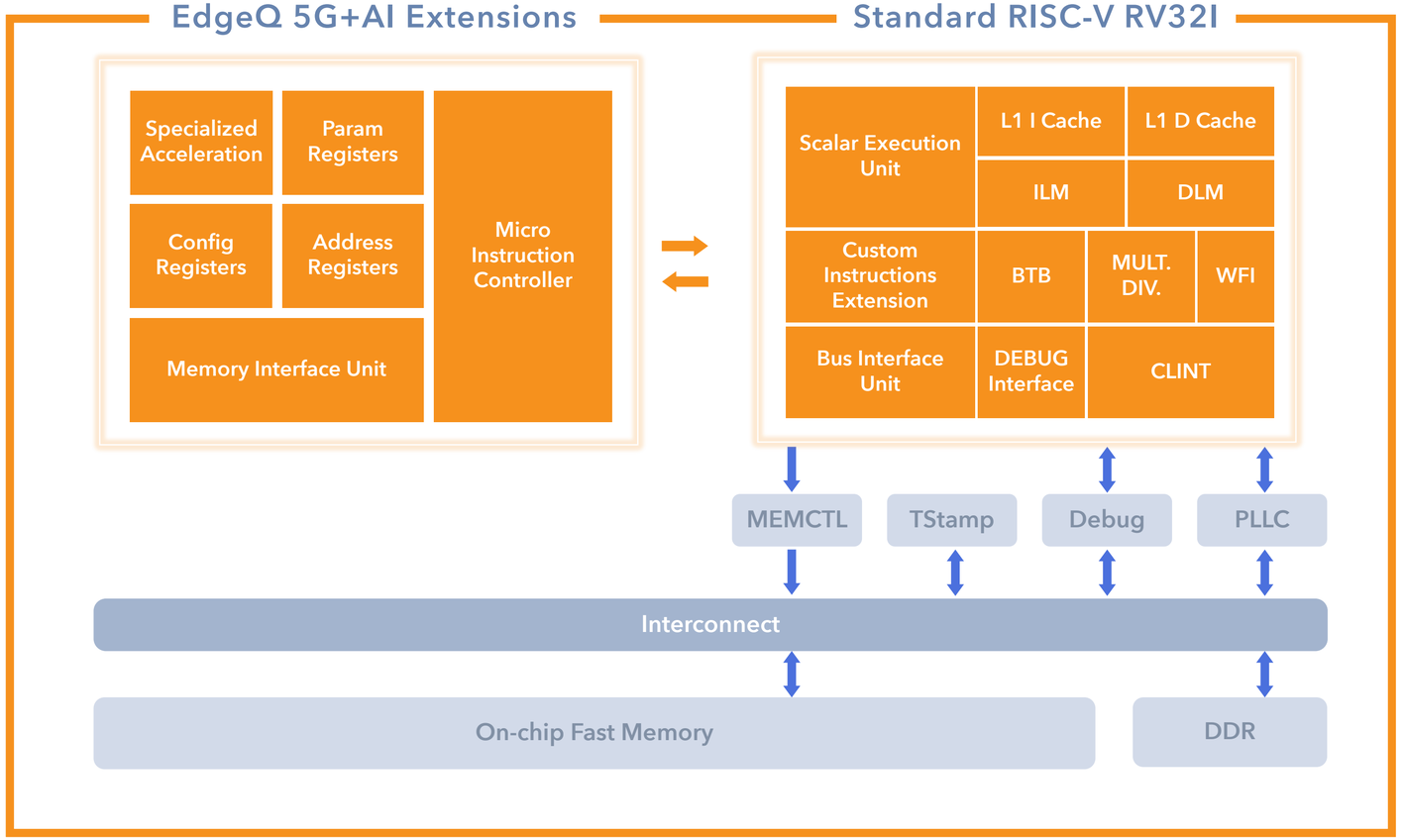
ADCs, DACs, and Up/Down Sampler Chains with Support for AGC/Channel Sense/Sigdet and DPD

MASSIVELY PARALLEL | FULLY PROGRAMMABLE | INTEGRATED (5G + AI + NPU + CPU) | GNU TOOL CHAIN

Heart of EdgeQ: The DSP Complex

- Multi-Core RISC-V Scaler Baseband
- Multi-Stage Arithmetic Unit and Register File Design
- Custom Instruction Extensions
- Scalable Numerology
- Converged Non-Linear Functions Approximator (for 5G and Machine Learning)





Converged 5G + AI Compute Cores

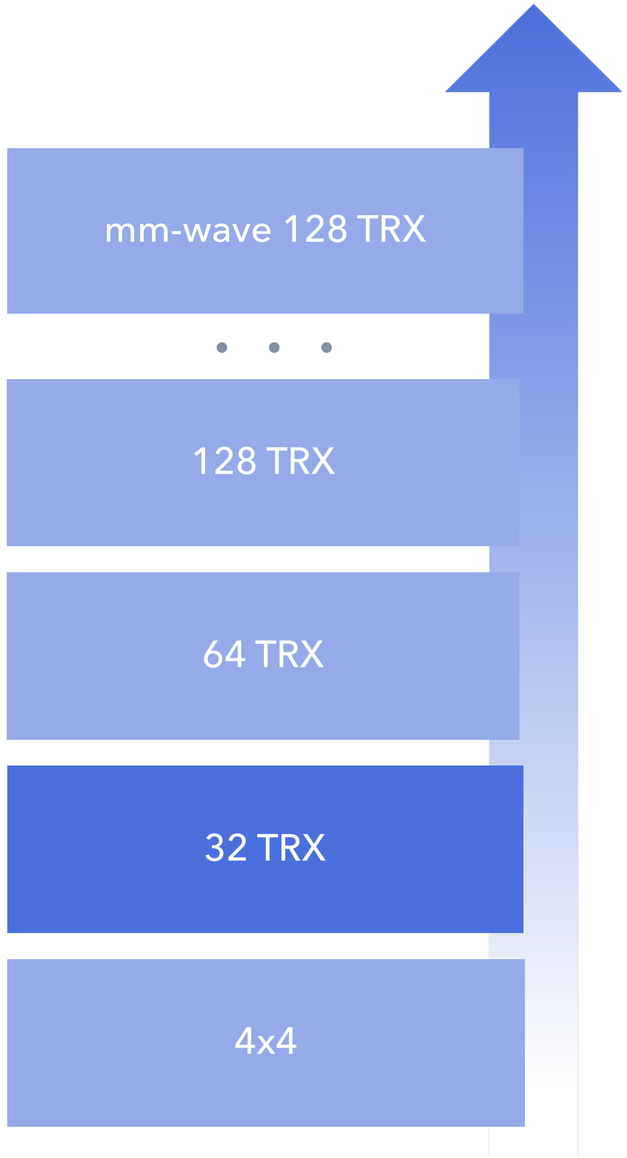
Singular Programmable Design

Dynamically Programmable for:
Radio Unit (RU) / Distributed Unit (RU) / Small Cell (gNB)

EdgeQ RISC-V with Baseband Extensions

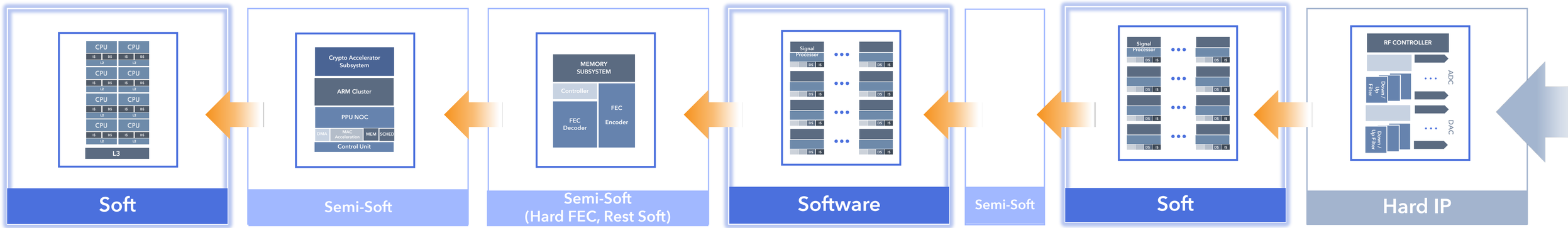
- FFT (Fast Fourier Transform)
- Complex modulations
- Non-linear functions
- Matrix Decompositions
- Equalization
- Function Specific Acceleration
- Multi-support for 4G/LTE and 5G/NR
- More …

EdgeQ 4G/5G DU Performance



Bandwidth	Throughput	# of EdgeQ	Carriers
1x400 MHz	5Gbps	1	1
2x100 MHz	20-40 Gbps	4	1-2
2x100 MHz	10-20 Gbps	2	1-2
2x100 MHz	5-10 Gbps	1	1-2
4x100 MHz	10 Gbps	1	4

5G RX Baseband Flow - “Life-of-a-Packet”



CPU
(Host OS)

Linux OS
MAC, RLC, PDCP Processing
RRM/RRC Processing
Ng Interface

Protocol Accelerator
(MAC/RLC/Crypto)

MAC Acceleration
RLC Acceleration

FEC
(Upper PHY)

FEC Encoding/Decoding
Layer De/Mapping
De/Scrambling
Constellation Mapping
LLR Generation

DSP Complex
(DU Lower PHY)

DMRS signal insertion
Channel Estimation
Equalization
Beamforming generation
Symbol / Slot-level scheduling

E-CPRI
(Front-haul)

ORAN synchronization
eCPRI packetization
UDP acceleration
Ethernet termination

DSP Complex
(RU Lower PHY)

Symbol Processing
CP removal,
FFT/iFFT
Symbol / Slot-level scheduling
Beamforming application
eCPRI Compression/ Decompression

RF Interface
(Sample Processing)

Analog to Digital Conversion
Timing Synchronization
Down/Up Converters
Sampling Rate conversion
DC offset correction
IQ Imbalance correction
CFR,DPD

EDGEQ

EdgeQ.

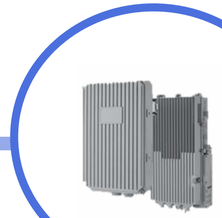
3 YEARS IN THE MAKING.
SAMPLING NOW

One Chip. Numerous Market Play

EDGEQ RADIO UNIT

EDGEQ DISTRIBUTED UNIT

EDGEQ 5G ACCESS POINT



vRAN / O-RAN Compliant | Software Programmable
Sub-6 and mmWave | Scales from Small to Macro Cells

SAMPLING.

THANK YOU.

EDGEQ