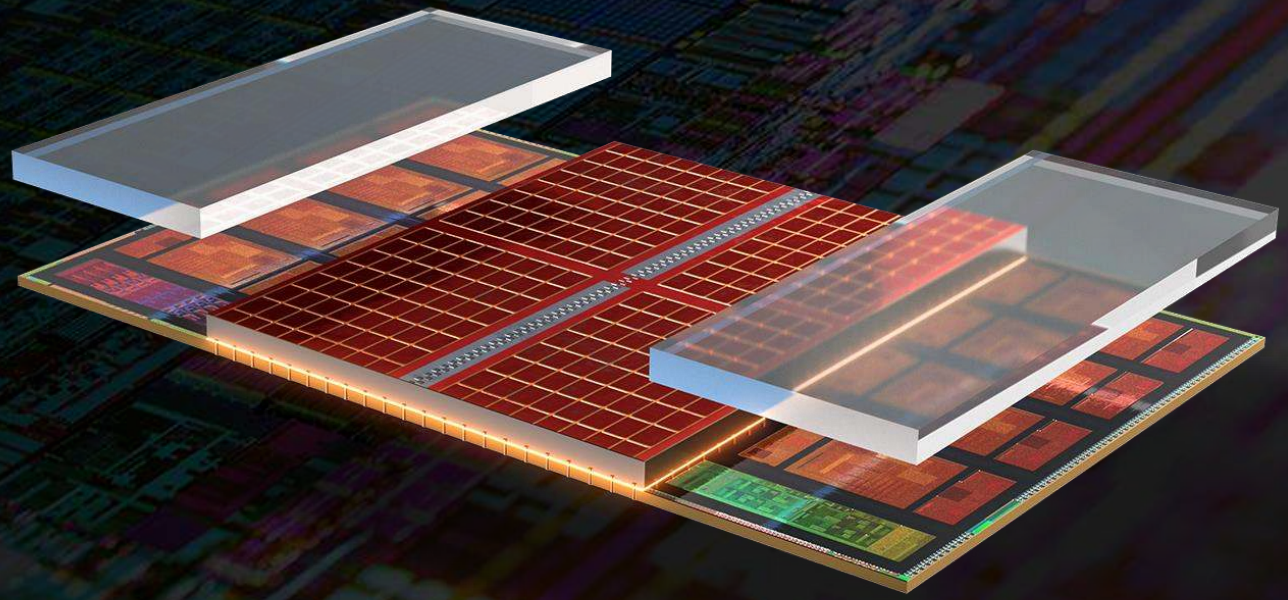
AMD

ADVANCED PACKAGING

ENABLING MOORE'S LAW'S NEXT FRONTIER THROUGH HETEROGENEOUS INTEGRATION



RAJA SWAMINATHAN

AMD SENIOR FELLOW &
ADVANCED PACKAGING LEADER

CAUTIONARY STATEMENT

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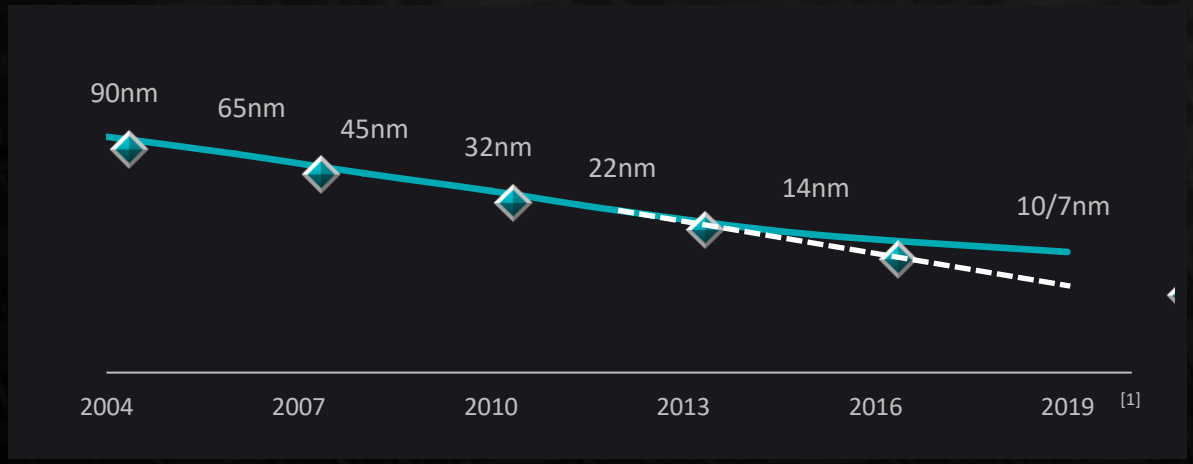
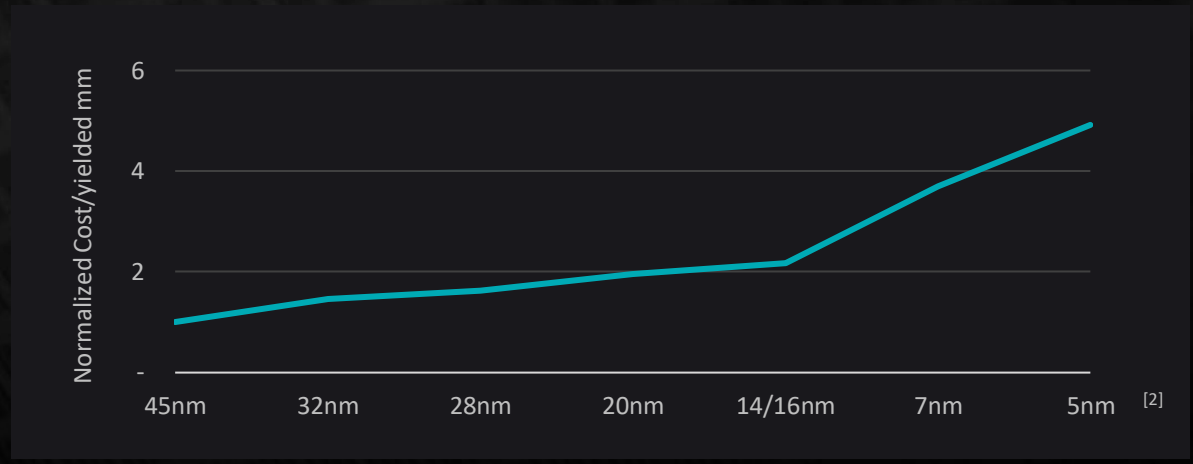
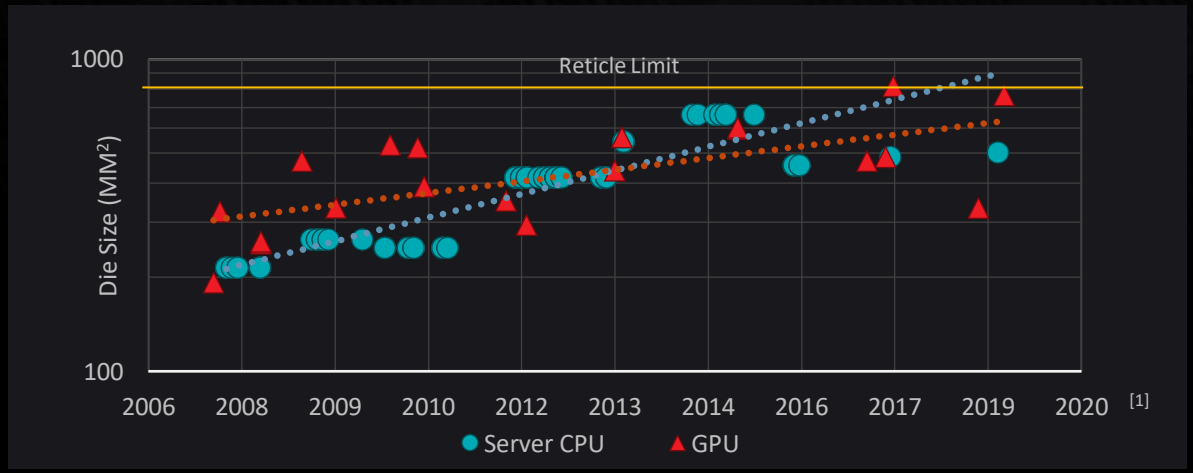
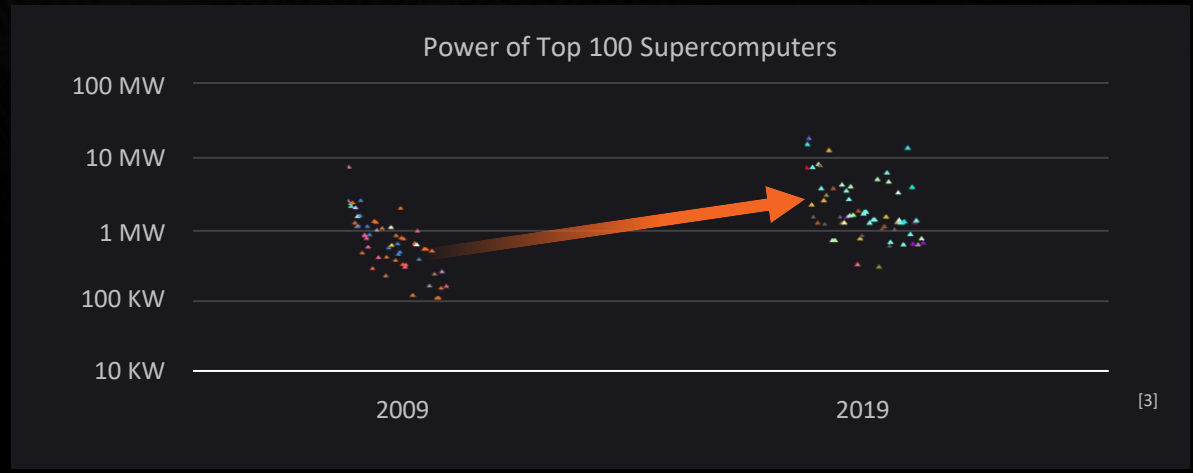
TECHNOLOGY CHALLENGES







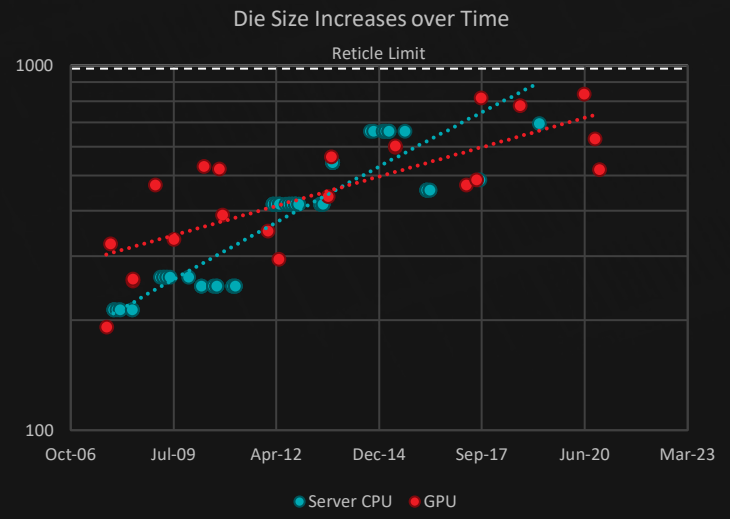


Many Well-known Technology Challenges | Slowing of Moore's Law, Cost Increases, Die-size Limits, Power

[1] Naffziger, VLSI Short Course, 2020, [2] Cost per yielded mm^2 for a $250mm^2$ die, [3] Data from top500.org

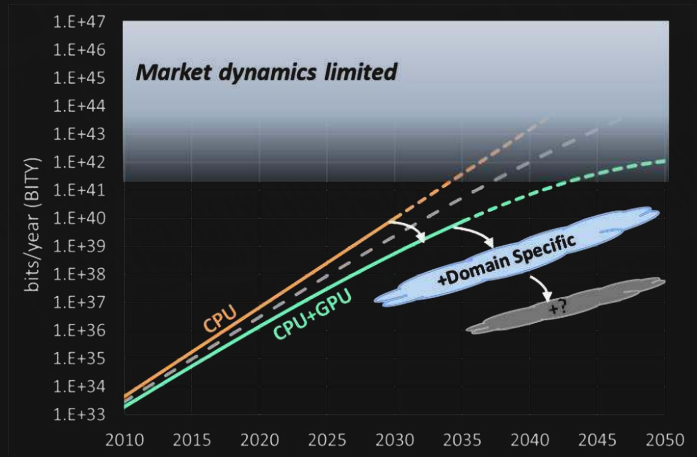
FUTURE OF COMPUTING

Compute Demand



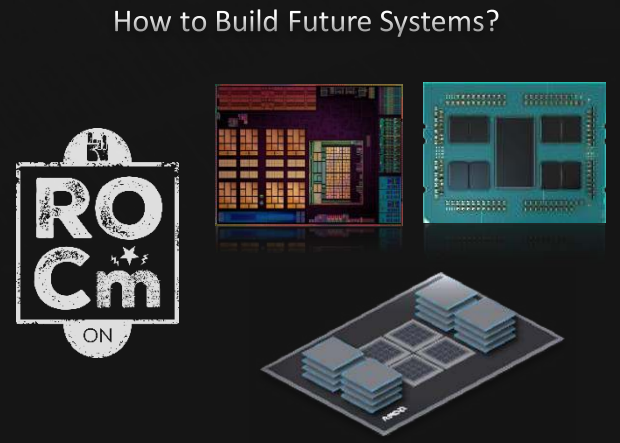
- Compute demand increasing
- Significant barriers to traditional scaling

Domain Specific Accelerators



- Higher efficiency domain specific accelerators required

Modular Design



- Modular design supported by advanced packaging required

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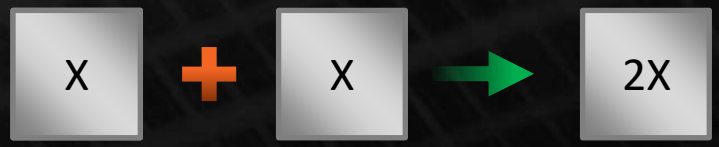
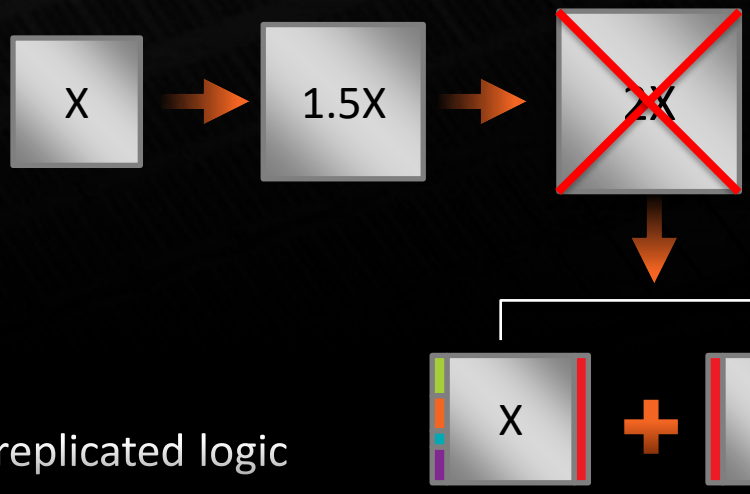
CHIPLETS BACKGROUND

Historically, except for the largest systems,
Moore's Law was sufficient to meet compute needs



One Generation Later

Current trends require a new approach



2X Device Functionality
Costs > 2X Silicon Area

However, chiplets not free

- Additional area for interfaces, replicated logic
- Additional design effort, complexity
- Past methodologies less suited for chiplets

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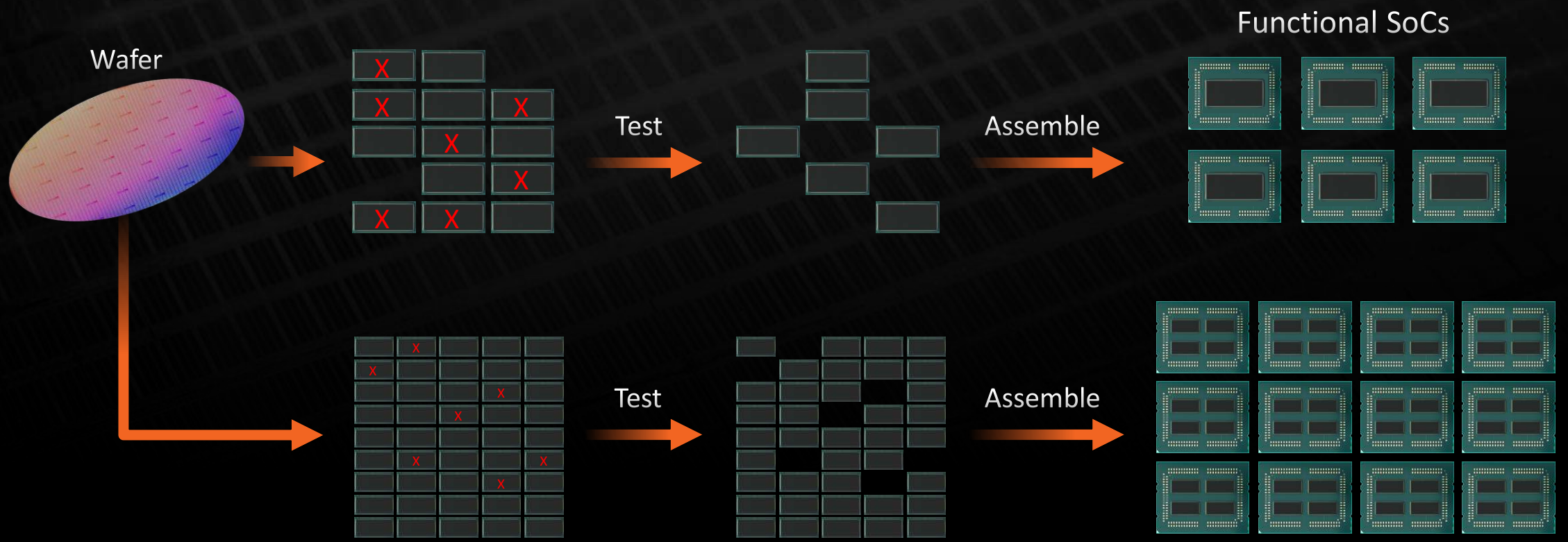
HIGH-LEVEL APPROACH TO CHIPLETS



Many More Functional SoCs

Ability to mix and match at a finer grained level

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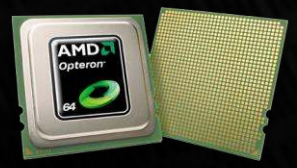
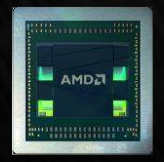
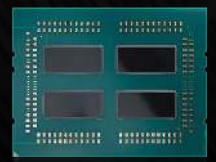
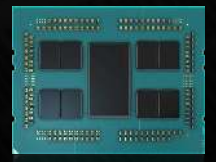
MODULAR DESIGN PROGRESSION

Earlier	2015	2017	2019	Future
MONOLITHIC DIE	2.5D HBM	MULTICHIP MODULE	CHIPLETS	MULTI-LAYER CHIP DESIGN



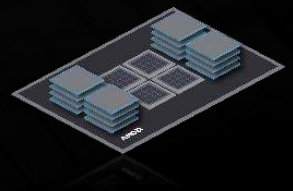






(Hybrid 2D/2.5D & 3D)

>10x
BANDWIDTH DENSITY



Key Parameters for Modular Chiplet Integration

- Cost and volume capability – addressing the world's compute needs requires scalable, cost-effective solutions
- Bandwidth density – area overhead of die-die communication must be minimized
- Energy per bit – tighter integration means more bits/s. Power cost must be minimized

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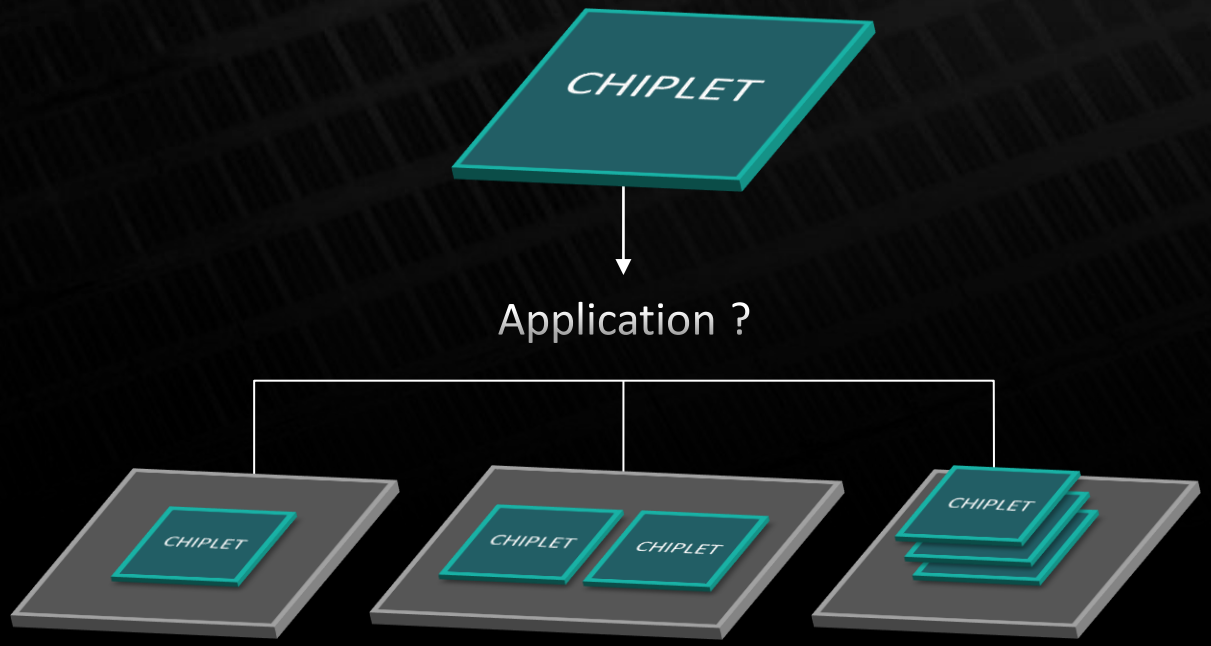
PACKAGE ARCHITECTURE GOALS

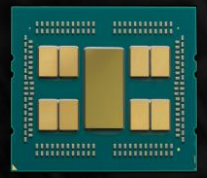
ENABLING A FLEXIBLE PACKAGING APPROACH



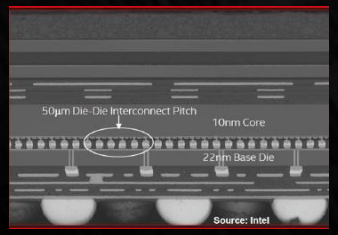
- Enable performance, power, area, cost (PPAC) for high-performance leadership products
- Heterogeneous architectures for configurable, segment-specific optimization
- Maximize product yield by enabling smaller, low-interconnect-overhead chiplets

PACKAGE ARCHITECTURES FOR CHIPLETS

MCM

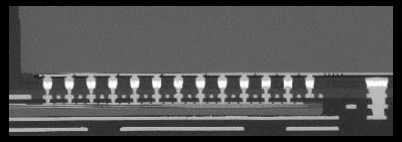


Foveros

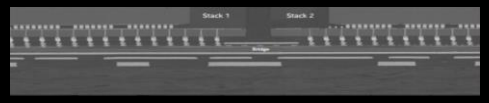


Intel: Foveros

EMIB

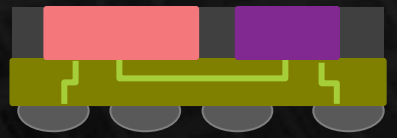


Co-EMIB

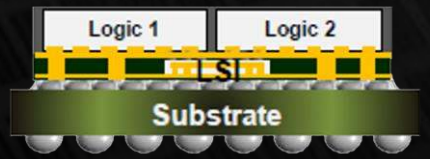


Intel: EMIB and Co-EMIB

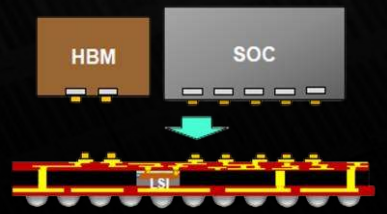
INFO-R



INFO-L

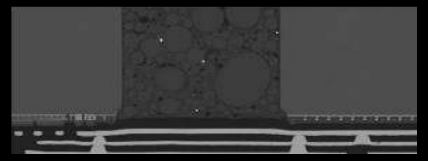


CoWoS-L



TSMC: INFO-R/-L, CoWoS-L

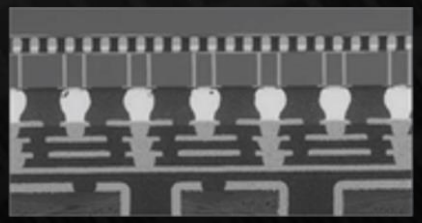
FoCoS



ASE: FoCoS

Micro Bump 3D

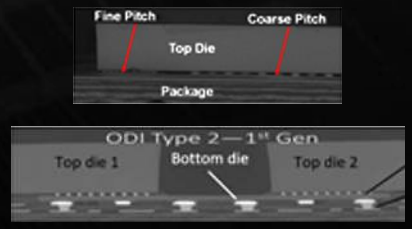
Si Interposer + TSV



AMD Fiji GPU

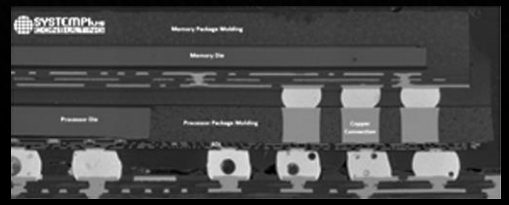
Courtesy: TechSearch

Foveros-ODI



Intel: Omni-directional interconnect

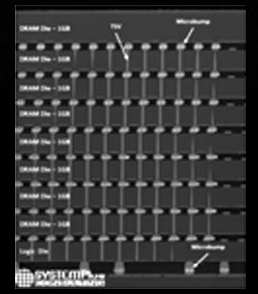
INFO-POP



Apple A10 on FO+POP

Courtesy: SystemPlus Consulting

W2W stacking+ TSV+uBump



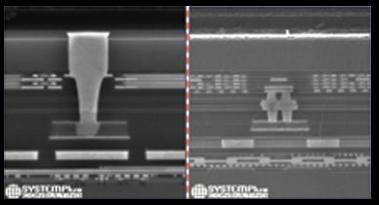
Samsung: HBM2 memory

Courtesy: SystemPlus Consulting

WoW

W2W F2F di-electric bonding+ TSV

W2W F2F hybrid bonding w/o TSV



Sony: CMOS Image Sensors

Courtesy: SystemPlus Consulting

No single package architecture works for all products - choice based on product PPAC

Images courtesy: Intel, TSMC, Amkor, ASE from public material

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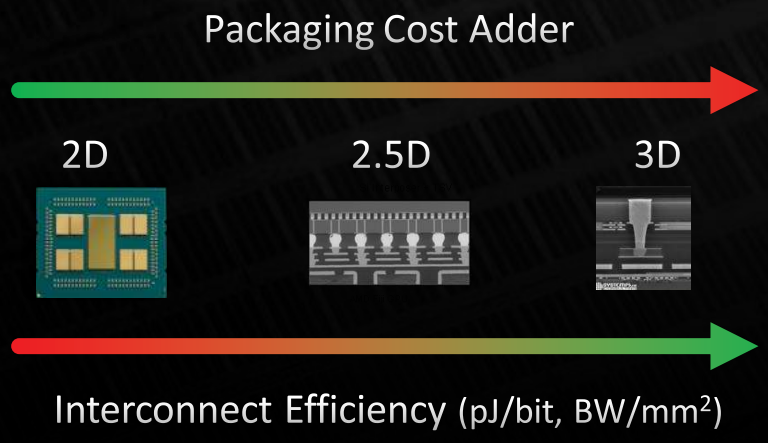
FINDING THE OPTIMAL SOLUTION

Chiplet package architecture selection requires balancing a complex equation…



[Value of modular product]
+
[Chiplet yield and technology cost benefit]

>

[Chiplet die overhead adder]
+
[Packaging cost adder]
+
[Power cost of interconnect]
+
[Engineering complexity of solution]

Architectural need for bandwidth, die partition options and package technology create a multi-disciplinary optimization equation

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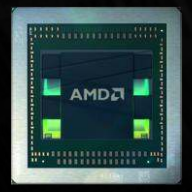
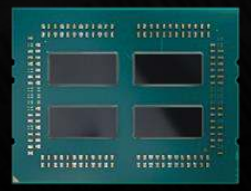
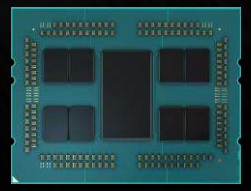
AMD LEADERSHIP PACKAGING

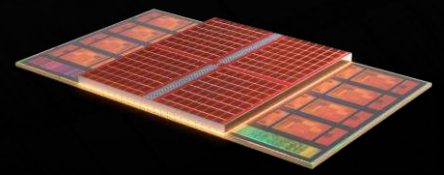
2015	2017	2019	2021
2.5D HBM	MULTICHIP MODULE	CHIPLETS	3D CHIPLETS







(Chiplet + Advanced 3D Stacking)



Led Industry in HBM, 2.5D & Chiplet Architecture

Aggressive Roadmap for Chiplet & 3D Integration

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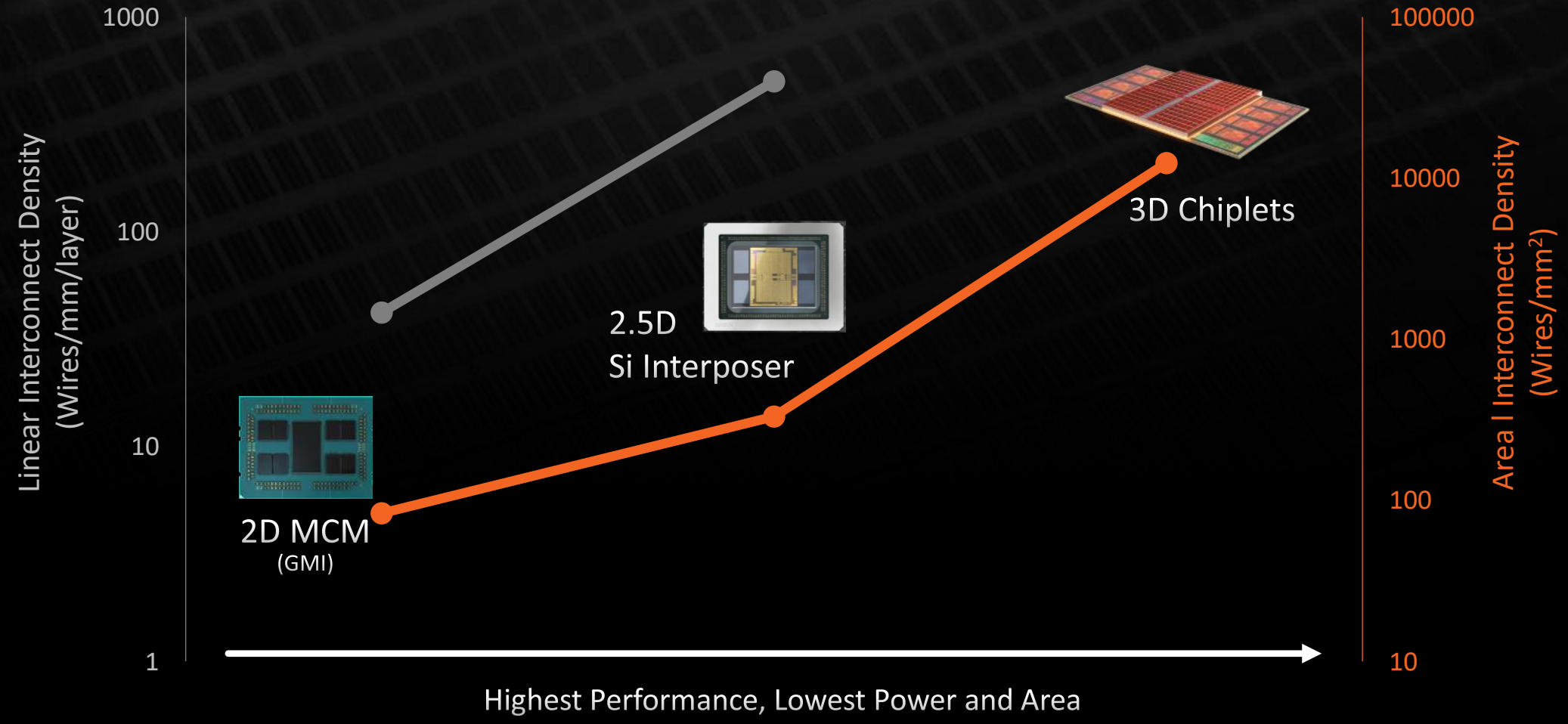
AMD PACKAGING ROADMAP



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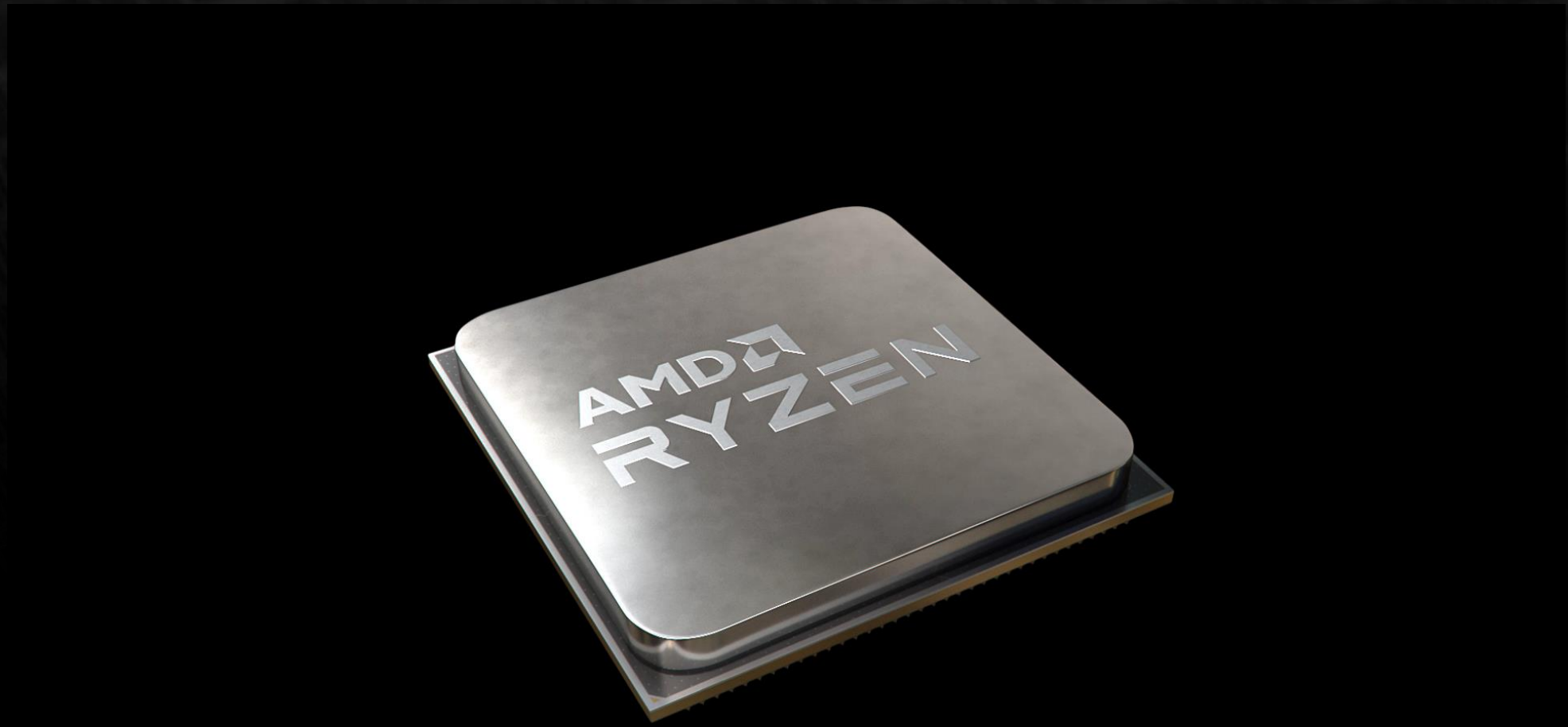
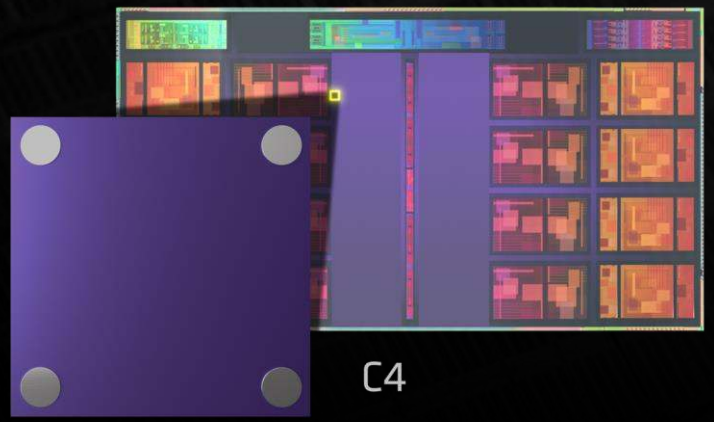
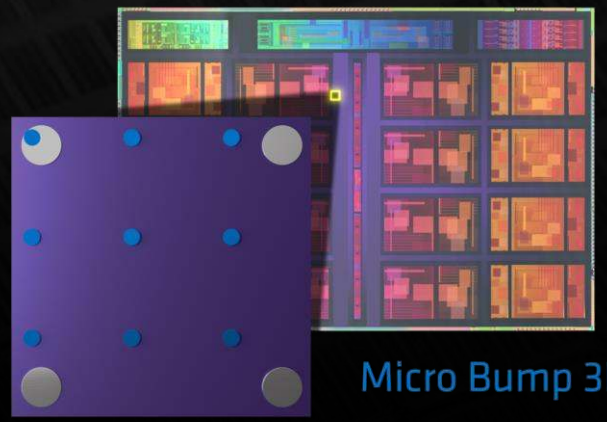
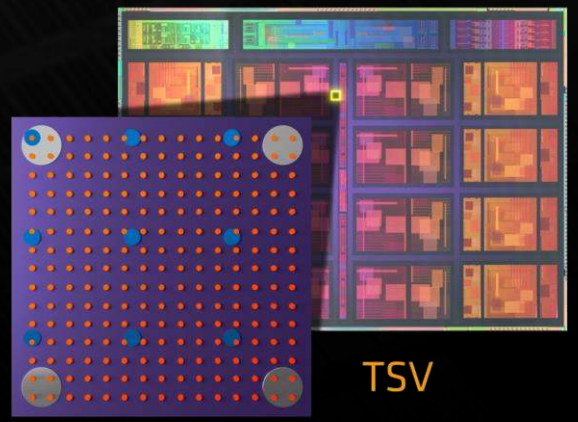
AMD 3D CHIPLET TECHNOLOGY



AMD 3D CHIPLET TECHNOLOGY

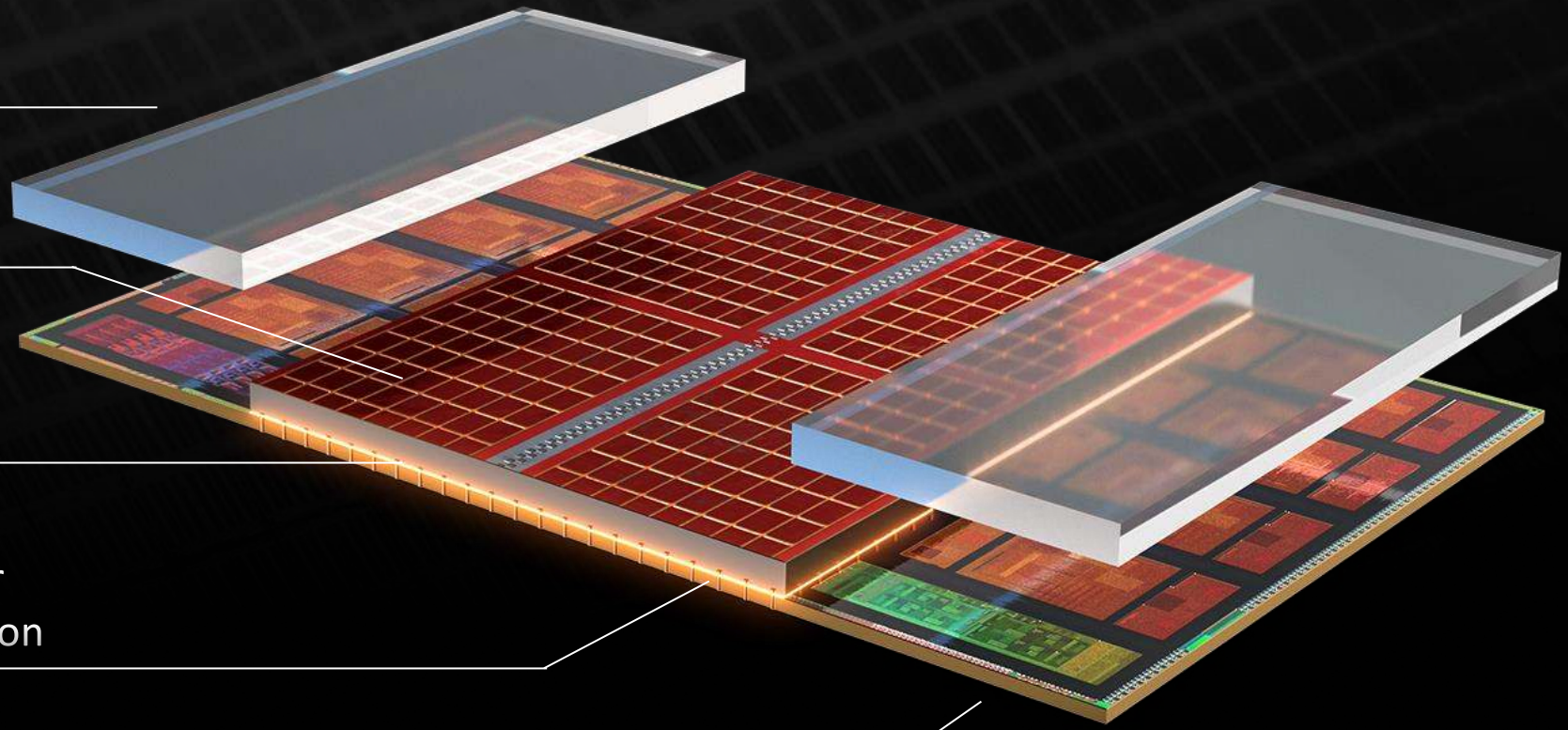






C4 and Micro Bump 3D illustrations are hypothetical

ENGINEERING THE 3D CHIPLET ARCHITECTURE



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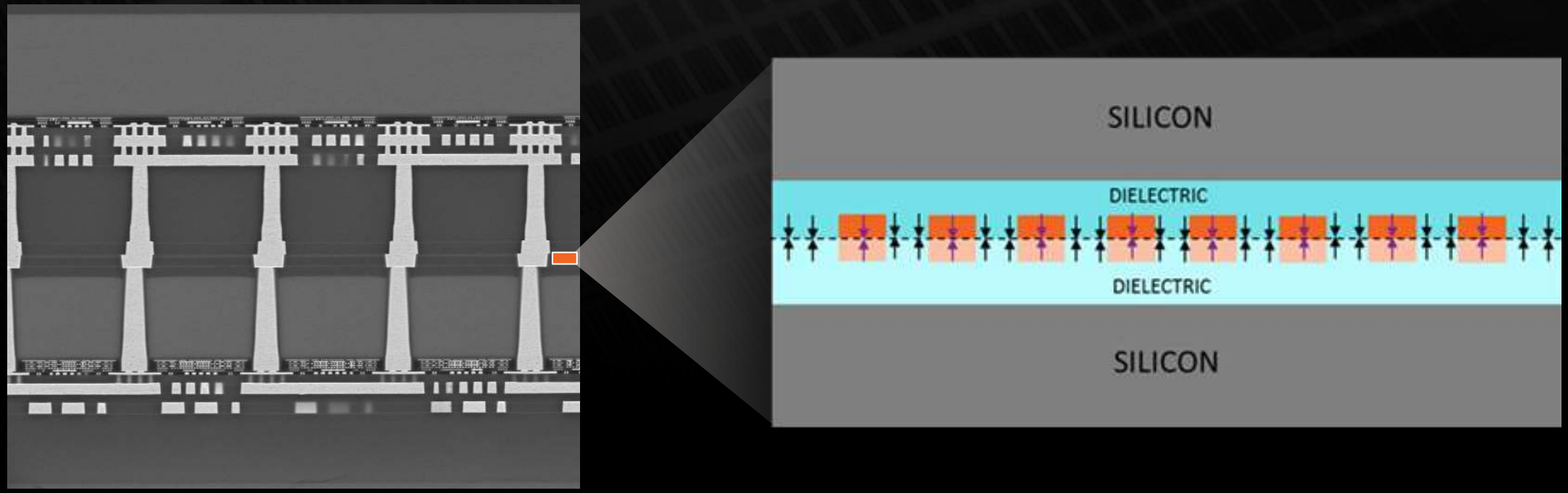
HYBRID BONDING

HYDROPHILIC DIELECTRIC-DIELECTRIC BONDING + DIRECT CU-CU BONDING



TECHNOLOGY/DESIGN CO-OPTIMIZED IN DEEP PARTNERSHIP WITH TSMC

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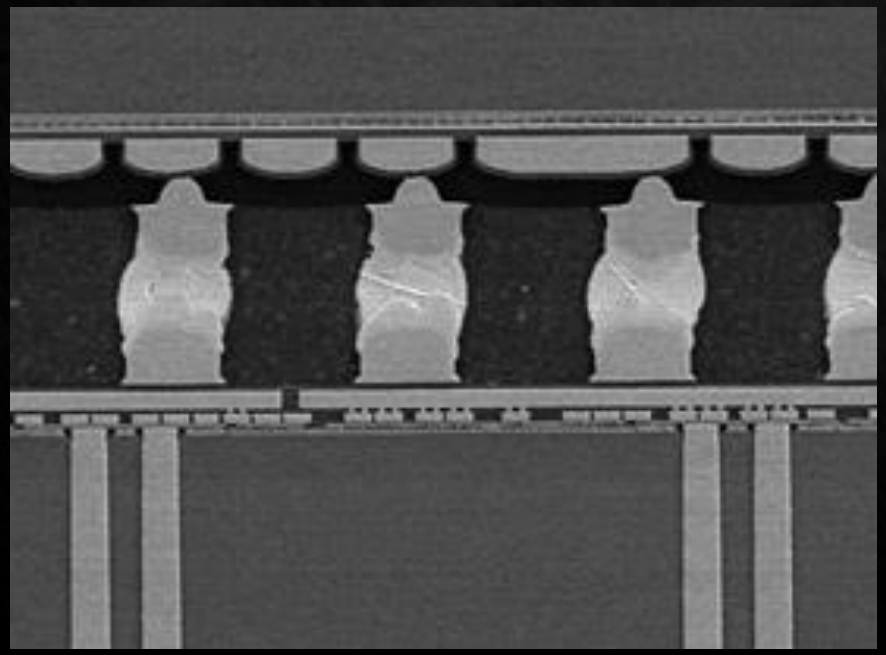
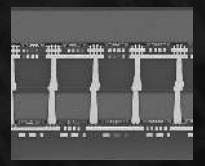
OTHER 3D ARCHITECTURE



Micro Bump (50u→36u pitch)

~50u tall TSV

AMD 3D CHIPLETS



Hybrid Bond (9u pitch)

Back End Like TSV

>3X

Interconnect Energy Efficiency

Compared to Micro Bump 3D

>15X

Interconnect Density

Compared to Micro Bump 3D

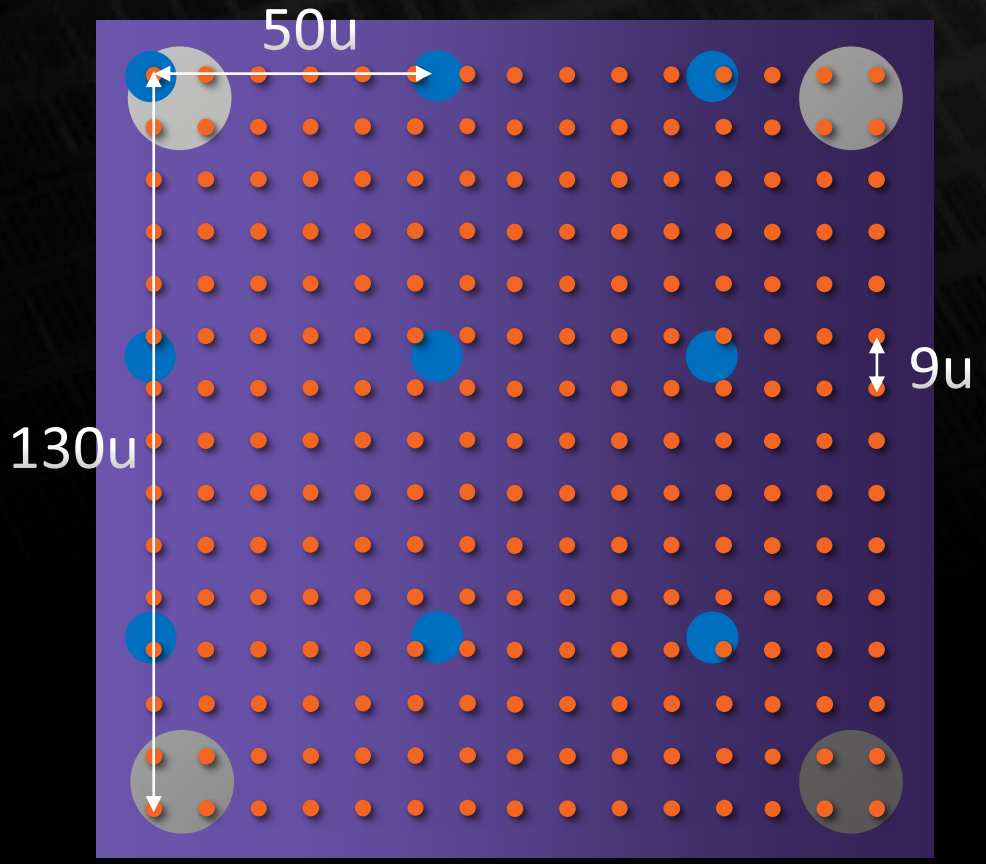
BETTER SIGNAL/ POWER

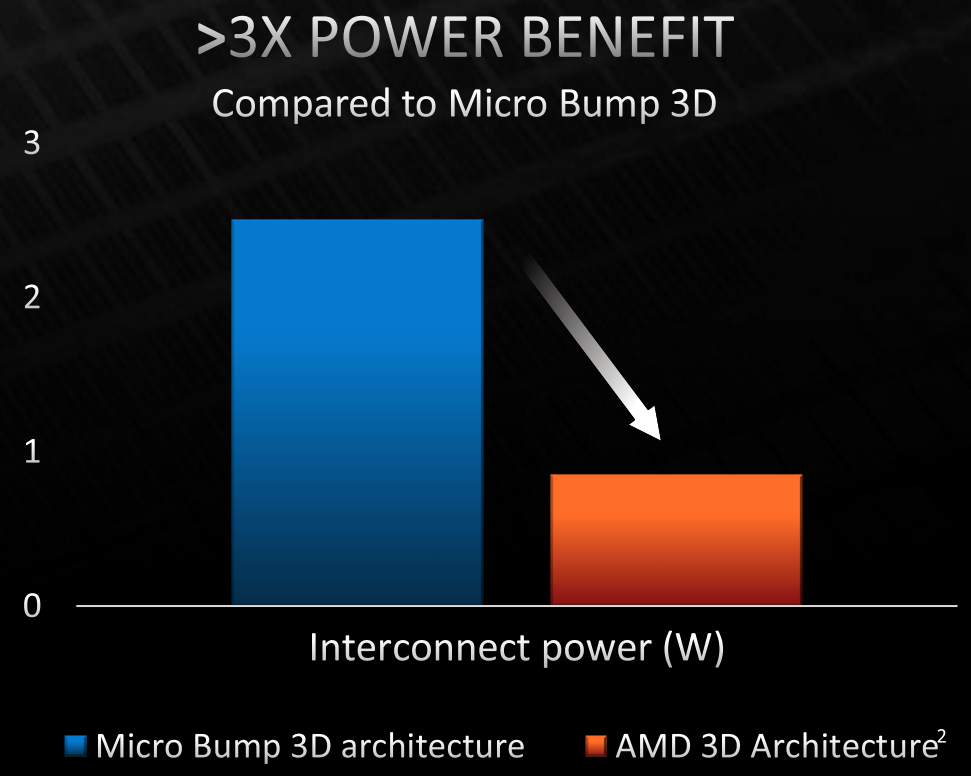
Lower TSV capacitance, inductance

Compared to Micro Bump 3D

Based on AMD engineering internal analysis, May 2021 See endnotes.

POWER AND AREA BENEFITS





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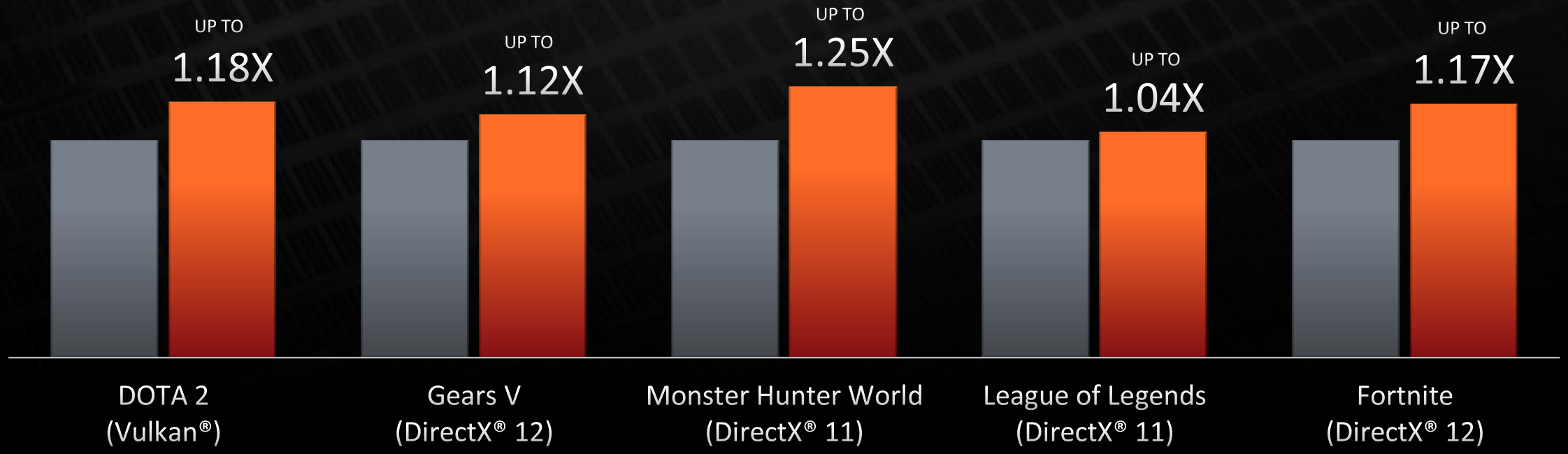
3D CHIPLET TECHNOLOGY

15% FASTER GAMING ON AVERAGE



ADVANCED PACKAGING ENABLING GENERATIONAL PERFORMANCE GAINS

Based on AMD engineering internal analysis, May 2021

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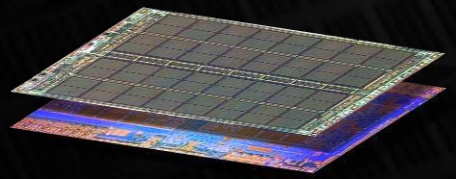
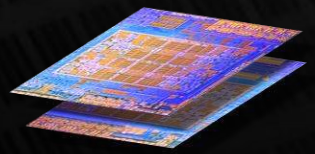
FUTURE OF 3D STACKING

TSV Pitch

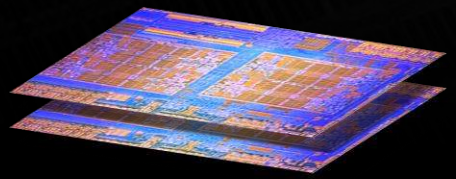
DRAM on CPU



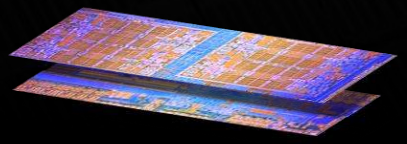
Cores on Cores



CPU on CPU



Cores on Uncore

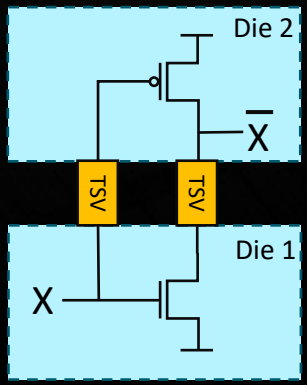


Full die-to-die

IP on IP

Macro on Macro

IP Folding/Splitting



Circuit Slicing

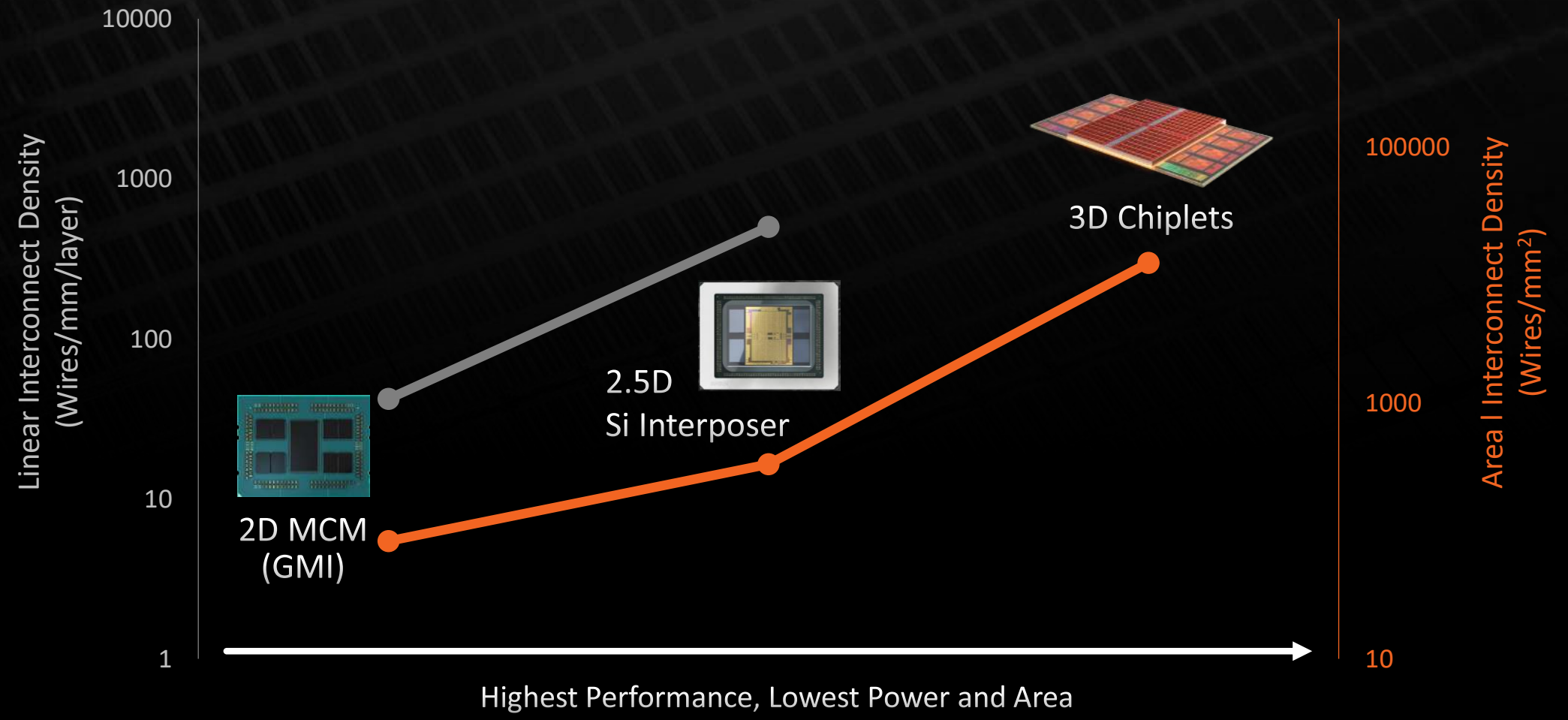
ADVANCED PACKAGING CAN ENABLE INTEGRATION SCHEMES
NOT POSSIBLE WITH MONOLITHIC DESIGNS

Based on AMD engineering internal analysis, May 2021

AMD

ACCELERATING WITH ADVANCED PACKAGING

DRIVING HIGH-PERFORMANCE COMPUTING FORWARD



AMD

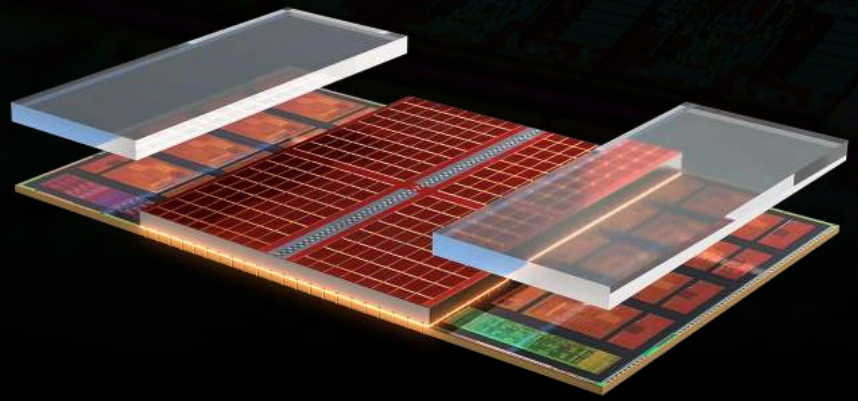
ACCELERATING WITH ADVANCED PACKAGING

DRIVING HIGH-PERFORMANCE COMPUTING FORWARD

SILICON PROCESS SLOWING → ADVANCED PACKAGING INNOVATIONS CRITICAL

AMD

ADVANCED PACKAGING LEADERSHIP



ENDNOTES

AMD 3D Chiplet Technology

Competition 3D architecture picture from SystemPlus. Intel Core i5-L16G7: the first utilization of Intel's Foveros Technology with Package-on-Package configuration in a consumer product.. https://www.systemplus.fr/reverse-costing-reports/intel-foveros-3d-packaging-technology/

3D Chiplet Gaming Demo And Performance Chart

Testing by AMD performance labs as of April 28, 2021 based on the average FPS of 32 PC games at 1920x1080 with the High image quality preset using an AMD Ryzen™ 9 5900X processor vs. 12-Core 3D Chiplet Prototype. Results may vary. R5K-078.

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